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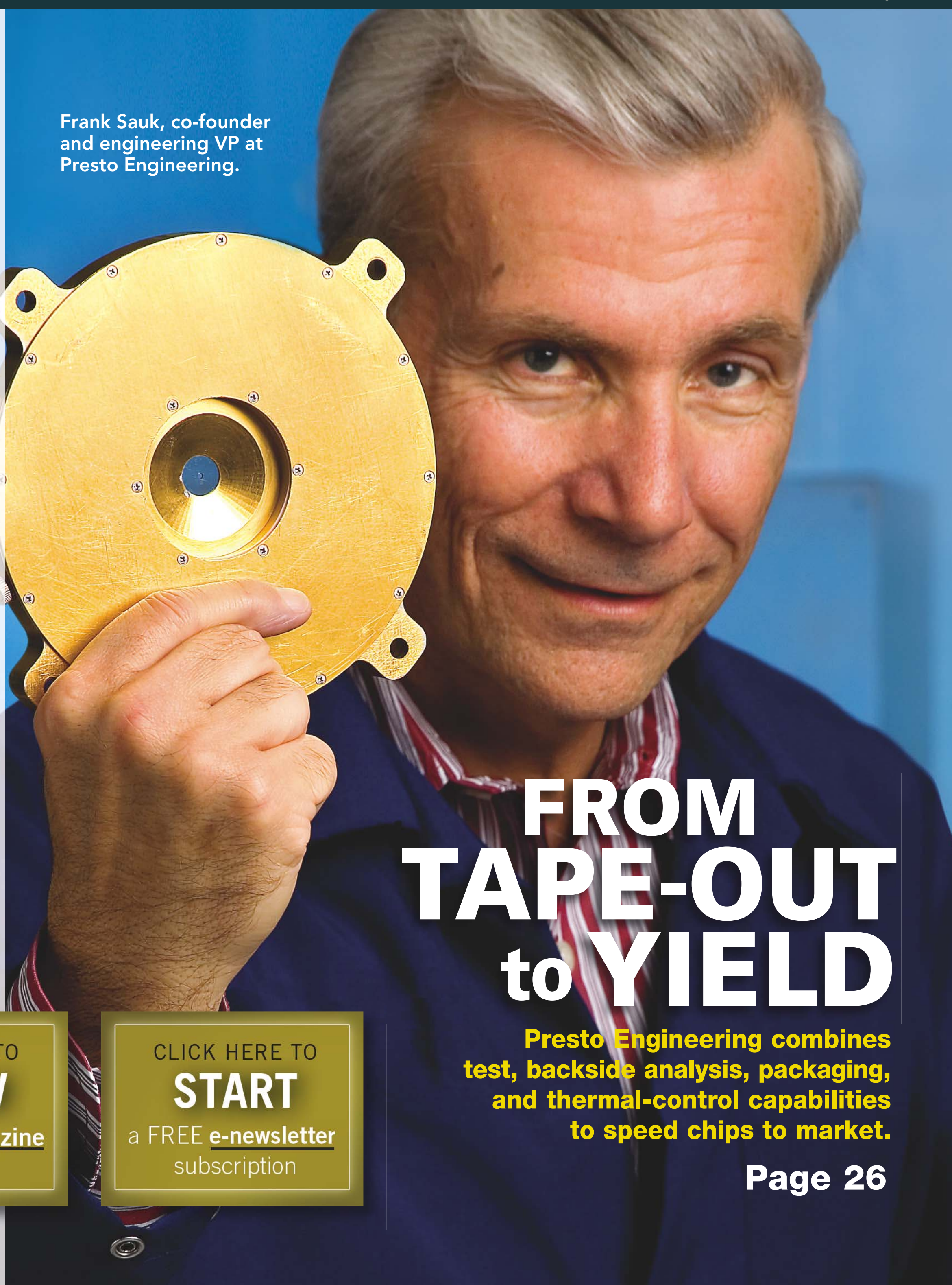

Frank Sauk, co-founder and engineering VP at Presto Engineering.

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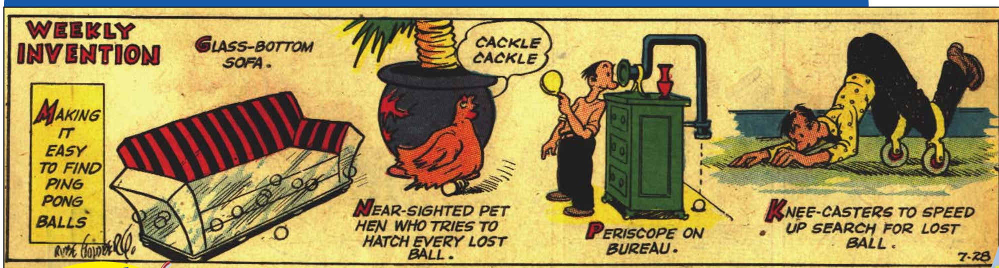

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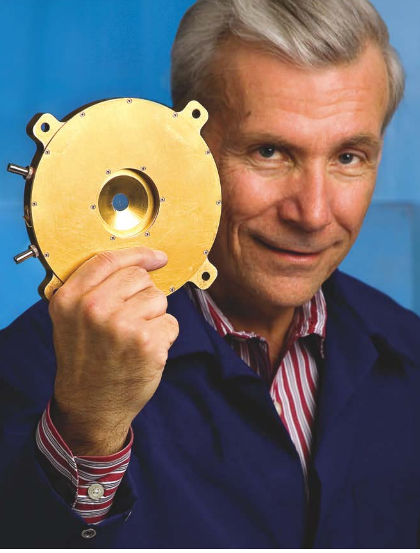

COVER BY: GARY LAUFMAN

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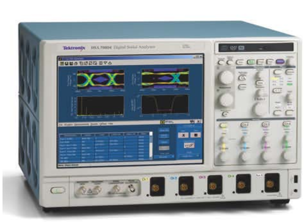

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Guest commentary

GPIB remains in heavy use

Murali Ravindran of National Instruments says that in the engineering world of unknowns, it is reassuring to know you can count on GPIB-based systems to function properly.

www.tmworld.com/guests

Inspecting the wafer test

Nathan Little of Rudolph Technologies contends that you can examine the marks left by wafer-probe cards to garner information about the quality of the test as well as about the 'goodness' of the prober.

www.tmworld.com/rudolph_wafer

Blog commentaries and links

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Martin Rowe, Senior Technical Editor

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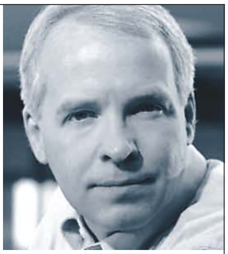

Green engineering matures

The green age has arrived. It has been heralded by *The Economist* in a January 17 article titled "A change in climate—the greening of corporate responsibility." Corporate responsibilities now seem to include addressing climate change and other environmental concerns, but along with the responsibilities come opportunities—in particular, *The Economist* states, opportunities for lofty rhetoric. The article quotes PepsiCo's Indra Nooyi stressing the need for companies to "contribute positively and responsibly to human civilization."

But there are practical opportunities as well. *The Economist* article also quotes United Technologies CEO George David as saying that in 30 years, conservation initiatives could account for 30% of the company's business, up from nothing today.

"Concerns about climate change, soaring energy costs, and government mandates are driving green engineering."

Even the US military is in on the game. The May 21 *Wall Street Journal* reports that Army engineers are pushing contractors to build hybrid armored vehicles, while the Air Force is experimenting with lighter-weight engine parts to boost fuel efficiency. In addition, the *Journal* reports, "Nellis Air Force Base near Las Vegas opened one of the largest solar arrays in the US, a 140-acre field of 72,000 motorized panels that powers the base and sells energy to nearby communities."

As organizations pursue green initiatives, measurement will play a key role. *The Economist* quotes Linda Fisher, the chief sustainability officer at DuPont, as saying, "We find with energy and greenhouse gases, if you start to measure, people reduce the usage."

One company that is capitalizing on the trend is National Instruments, according to NI industrial group manager Joel Shapiro. In a phone interview, Shapiro, who defines green engineering as the process of using measurement and control techniques in the design, development, and improvement of products to yield environmental and economic benefits, said that three factors are leading the emphasis on this discipline: first, concerns about climate change; second, soaring energy costs; and third, the need to comply with government mandates. With regard to mandates, Shapiro said that 50 countries, including 13 developing countries, have some form of environmental legislation or incentive programs in place.

Not surprisingly, NI is touting its products as ones that can help the green-engineering movement. Applications in which NI has provided products, Shapiro said, include environmental monitoring at the La Selva Biological Station in Costa Rica and, for Madrid-based Energy to Quality, fault-injection tests that enable wind turbines to remain connected to the grid when most needed. He also cited Nucor Steel Marion, which made use of green engineering techniques to save energy in a facility that turns scrap into rebar. Shapiro cited Dave Brandt, an engineer at Nucor, as agreeing with DuPont's Fisher. "Once you start monitoring something in an automation system, you can fix things," Shapiro quoted Brandt as saying.

Efforts to bring wind turbines online and to improve the efficiency of steel mills might seem to offer the biggest opportunities for green engineering. But Shapiro said NI is also focusing on less obvious opportunities—such as the measurement of vampire currents, which household appliances can draw even when not turned on, running up significant electric bills. T&MW

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Test & Measurement World

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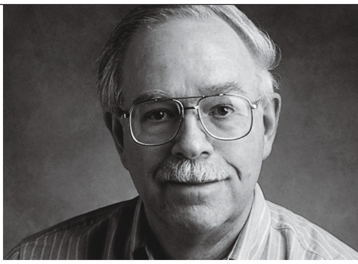


Opaque Windows

In his *Test & Measurement World* blog for April 14, 2008, my colleague Martin Rowe suggested that our readers should sign a petition requesting that Microsoft extend support for Windows XP past the published cutoff date of June 30, 2008. Created by InfoWorld, the petition so far has accumulated more than 180,000 signatures but will probably have all the impact of a June bug hitting Microsoft's windshield.

Having spent the better part of a week resurrecting my PC and reinstalling Windows after a complicated failure cascade involving a motherboard problem that caused a hard-disk crash in a RAID-1 array, accompanied by unexplainable damage to the master hard drive's Windows system image, I'm not in the mood to adopt Microsoft's latest offering.

My last contact with a Microsoft operating system's innards occurred with CP/M, which I vaguely understood and could modify to meet the hardware needs of various systems from the mid-1970s. I had to understand CP/M because I had no choice, but it wasn't that onerous a process in spite of Microsoft's opaque documentation.

Today, my PC provides me with a workspace, a toolkit, and test-instrument control. I shouldn't have to care about what's going on inside the operating system nor worry about anything except the work that I'm performing. And I can't afford to replace certain older software packages that Windows Vista won't support.

In an ideal world, Microsoft's next operating system would feature improved (and understandable) error messages, modular design, and detailed diagnostics that locate and facilitate replacement of damaged parts of the operating system. Put another way, the PC and its operating system should resemble a full-featured oscilloscope. If half of a scope's screen goes blank, you can consult a troubleshooting manual and check various things—connectors, power-supply voltages, and circuit subassemblies—to isolate the failure to a particular subcircuit or component.

Does any Linux version or the current Macintosh operating system appear logically designed and easier to troubleshoot? I doubt it, but I'm experimenting with Linux. In the meantime, I'll continue to use Windows 2000 and build on my understanding of its failure modes and foibles. But I'm not interested in starting anew with yet another Microsoft operating system. T&MW

IT'S SPRING—TAKE A HAIKU

To read Martin Rowe's blog posting, "Test engineers should vote to save Windows XP," go here:
www.tmworld.com/blog/1430000143/post/1190024919.html

To sign InfoWorld's petition, go here:
weblog.infoworld.com/save-xp

Are you fed up with Windows' cryptic error messages? Consider alternative forms such as these haiku error messages:
baetzler.de/humor/haiku_error.var

And while you're at it, try writing haiku for your test instruments. Here's an example:

Last week's waveform
Darkens the phosphor.
Next time, reduce intensity.

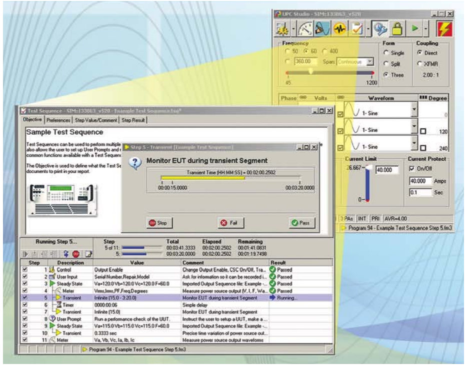
For a primer on writing haiku, go to:
baetzler.de/poetry/lexa_haiku_def.html

Spring has arrived here in the northern hemisphere, and this cartoon reminds us of what's important:
xkcd.com/227

Back to work: If you're at all involved with RF design and test technology, chances are you'll find a useful utility, or at minimum valuable pointers to other helpful Web sites, via Green Bay Professional Packet Radio's voluminous Web site. Plan on spending at least a half hour browsing through the site:
www.qsl.net/n9zia

Unless you work in the oil industry, you may never encounter truly high-temperature applications for electronics. Even if you can comfortably press your fingers against your product's heat sink, a visit to this Web site will prove educational (and entertaining—see "The Tallini Tales of Destruction"):
www.logwell.com

Test-management software controls AC power sources



Pacific Power Source has added a Test Manager feature to its UPC (Universal Programmable Controller) Studio Version 1.3 graphical software tool for controlling the vendor's line of AC power sources. UPC Studio Test Manager helps users create and run test sequences and test plans. The new release's test-sequences feature is designed to execute a series of automated tasks that control and monitor an AC power source and other instruments. The test-plans feature allows a user to link together a series of test sequences by using prompts, user controls, Visual Basic scripts, and other techniques.

With Test Manager, the user can automate instrument compliance testing as well as obtain preconfigured test sequences and test plans from the vendor, including sequences that support avionics compliance testing in accordance with MIL-STD-704 and RTCA DO-160. Test Manager complements other features such as a waveform editor, the ability to measure and graph voltage and current harmonics to customer-specified limits, and the ability to provide control of transients within output sequences. In addition to controlling an AC power source, UPC Studio can be used to generate and view offline simulation files, enabling a user to observe steady-state waveforms and programmed transients before applying power to the equipment under test.

The basic UPC Studio is free. Activation of the Test Manager feature costs $1750, and factory-written test sequences start at $500. www.pacificpower.com.

Mentor Graphics announces partnership with NXP for DFT

Mentor Graphics has announced a partnership with NXP Semiconductors in which NXP will use Mentor's design-for-test (DFT) products, including the TestKompress compressed-pattern-generation and Yield-Assist failure-diagnosis tools, to improve the quality and time-to-market of NXP's products. The agreement also provides interim support for NXP's test tools.

Under the agreement, Mentor Graphics also obtains rights to NXP's internally developed test tools, technology, and talent as a portion of NXP's DFT tools-development organization joins Mentor's design-for-test product division. This division of Mentor is also establishing a new R&D facility in Hamburg.

"We're excited about our new business relationship with NXP. It not only brings new DFT technology to Mentor, but also brings the talent of world-class DFT developers, which will help us accelerate the development and delivery of innovative DFT technologies into the marketplace," said Joe Sawicki, VP and GM of the design-to-silicon division at Mentor Graphics. "We expect the partnership to produce dividends for both parties and ultimately to create value that can be passed on to all Mentor DFT customers." www.mentor.com; www.nxp.com.

Renesas chooses J750 for microcontroller test

Teradyne has announced that Renesas Technology has standardized on using the Teradyne J750 platform for micro-

Editors' CHOICE

Cascade debuts integrated flicker-noise-measurement system

Cascade Microtech has introduced the Edge system, which is designed to measure the flicker, or 1/f, noise that occurs in all semiconductors and can compromise device performance by causing jitter or phase noise in communications devices. Able to make measurements from 1 Hz to 30 MHz, the Edge flicker-noise-measurement system integrates a wafer-probe station, an Agilent Technologies 4156 semiconductor parametric analyzer, an Agilent digital signal analyzer, software, and accessories.

The Edge system provides simple access to flicker noise data over its 30-MHz bandwidth while minimizing background noise, typically keeping it less than 1.2 nV/$\sqrt{Hz}$ at 100 kHz and above. In addition, it can switch between flicker and DC measurements with pushbutton automation, providing both sets of measurements over temperature in one system, eliminating risky transfer of a wafer from one measurement station to another.

Base price: $1.2 million. *Cascade Microtech, www.cascademicrotech.com.*

controller test at Renesas Semiconductor (Beijing). As a result of the standardization, Renesas, a joint venture of Hitachi and Mitsubishi Electric formed in 2003, will augment the number of J750 platforms it already uses for volume production in China and Japan. Renesas will use the additional J750 platforms to test microcontrollers used in automotive, consumer, communications, and industrial applications. www.teradyne.com; www.renesas.com.

ITRI chooses Agilent platform for WiMAX deployment

Agilent Technologies has announced that Industrial Technology Research Institute (ITRI) will use Agilent's E6474A wireless network test platform for its M-Taiwan WiMAX Applications Lab (MTWAL), a WiMAX Forum applications lab. Six operators in Taiwan that won WiMAX operating licenses last year are expected to roll out their networks and provide commercial services in the second half of 2008. ITRI will use Agilent's WiMAX test systems to support this rollout. Dr. Ching-Tarng Hsieh, engineering director of the Information and Communications Laboratories at ITRI, said that ITRI will use the E6474A to monitor quality-of-service information during the deployment of WiMAX technology. www.agilent.com; www.itri.org.tw.

CALENDAR

Semicon West, July 14–18, San Francisco, CA. Sponsored by SEMI. www.semiconwest.org.

IEEE EMC Symposium, August 18–22, Detroit, MI. Sponsored by the EMC Society of the IEEE. www.emc2008.org.

Autotestcon, September 8–11, Salt Lake City, UT. Sponsored by the IEEE. www.autotestcon.com.

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Editors' CHOICE

Develop your own microwave switch

VTI Microwave, a unit of VXI Technology, now lets you use its EX7000-OEM digital I/O unit as the heart of a custom RF/microwave switch system. The EX7000-OEM contains an LXI Class A-compliant Ethernet port and a digital I/O port for driving relays. You can integrate the digital I/O unit into any of several enclosures and then build a switch matrix using your own discrete relays, connecting them to the EX7000-OEM digital I/O lines, or you can use switches from VTI Microwave. For example, you can integrate the EX7000 into an EX725 chassis and populate the chassis with cylindrical multipole microwave switches. You then control the switches with a PC connected to the module's Ethernet port.

Before building your switch matrix, you can select parts and configure your matrix online, generating wiring lists and bills of materials. Then, you can download your configuration into the EX7000-OEM. Once the module is programmed with a configuration, its Web server sends you a graphical representation of the switch matrix and you can set switches with a browser. Because it is LXI Class A-compliant, the EX7000-OEM has IVI instrument drivers that let you control your switches under program control.

Prices: EX7000-OEM—$3500; enclosures—$3500–$4500. *VTI Microwave, www.vtimicrowave.com.*

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Oscilloscopes support the video craze

Flat-panel TVs now appear everywhere, from homes to supermarkets to airports. Appliances may soon have LCDs that replace knobs and buttons. All of this equipment needs a data interface, and the high-definition multimedia interface (HDMI) port is fast becoming the digital video interface of choice.

Market-research firm In-Stat reports that millions of HDMI ports have already shipped, and the number of shipments is expected to increase each year (**figure**). Because these ports are used in products such as TVs, DVD players, Blu-ray players, set-top boxes, and video games, interoperability among manufacturers is an issue. Consequently, the HDMI Consortium (www.hdmi.org) has developed compliance test specifications designed to minimize interoperability problems, and oscilloscope makers Agilent Technologies, LeCroy, and Tektronix have developed hardware and software to automate HDMI physical-layer compliance testing.

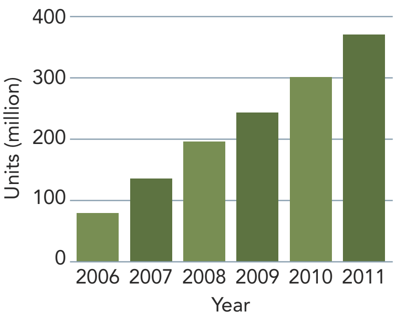
HDMI signals now run at speeds up to 3.4 Gbps based on HDMI specification 1.3, which was released in June 2006. The HDMI Compliance Test Specification (CTS) version 1.3b specifies test equipment and physical-layer performance limits for sources (transmitters), sinks (receivers), and cables. "Because HDMI specification 1.3 increased the data rate, the CTS needed to specify higher bandwidth oscilloscopes for compliance testing," said Faride Akretch, marketing manager for high-speed serial applications at Tektronix.

Because HDMI is a high-speed digital serial port, it falls victim to the usual set of signal-integrity problems: timing jitter, rise and fall time, noise, and signal loss. Source testing includes clock jitter, duty cycle, overshoot, rise and fall time, eye-mask tests, and inter-pair skew. For eye-diagram tests, you need to capture at least 2.6 million unit intervals when testing high-resolution devices.

Sink tests require a signal source such as a pattern generator and a jitter source. You must test for jitter tolerance, intra-pair skew, and differential voltage swing. Cable tests require a sampling oscilloscope with a time-domain reflectometer to measure S-parameters and cable loss.

Just because the HDMI specification version 1.3 specifies a data rate of 3.4 Gbps—double the rate specified by HDMI 1.2—doesn't mean that a device actually pushes data at that rate. Because most products with HDMI ports are consumer devices, cost is always an issue. HDMI 1.3 was a technology disruption because of its jump in data rate, said Brian Fetz, high-performance oscilloscope product manager at Agilent Technologies. "Engineers must design with inexpensive materials. They are trying to push data across standard FR4 PCB material, and the highest data rate running today is about 2.6 Gbps."

Even with compliance tests and approved test equipment, HDMI products may not interoperate. "Some interoperability problems occur even if a product is in compliance," said Akretch. "The specification writers may have not foreseen some behavior, and they may have to adapt the specification." Interoperability cases between compliant products, are rare, he added. T&MW



Shipment of goods with HDMI ports will continue to grow. Source: In-Stat.

FOR FURTHER INFORMATION

"HDMI/DVI," Tektronix, www.tek.com/Measurement/applications/serial_data/hdmidvi.html.

"HDMI Licensing Knowledge Base," www.hdmi.org/learningcenter/kb.aspx.

For inter-skew and intra-skew waveforms, see "Protecting the HDMI interface," by Jeff Donnihoo, Video Imaging Design Line, July 16, 2005. www.videsignline.com/165702853?pgno=2.

Video group approves test apparatus

The Video Electronics Standards Association (VESA) has approved the Tektronix DSA70804 8-GHz real-time oscilloscope with DPOJET Advanced software for DisplayPort compliance testing. DisplayPort is a high-speed serial link for transmitting video from computers to monitors. www.tek.com/displayport.

Integrated HDMI test system

Agilent Technologies has integrated control of the Quantum Data Model 882 video test instrument into its N5990A test automation platform. The N5990A performs physical layer tests while the Model 882 adds video protocol testing. www.quantumdata.com; www.agilent.com/find/HDMI.

Digital attenuator connects through USB

The LDA-102 and LDA-602 Lab Brick attenuators from Vaunix Technology cover 0.1 to 1000 MHz and 6 to 6000 MHz, respectively. Each model can attenuate signals by up to 63 dB with programmable step sizes from 0.5 dB to 63 dB. The attenuators are controlled and powered by a USB port. www.labbrick.com.

[AUTOMATED TEST EQUIPMENT]

S. VIDYASANKAR
INDUSTRY ANALYST
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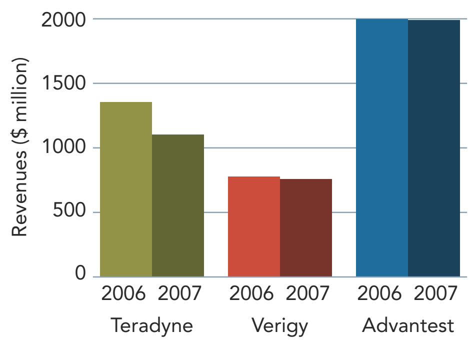
Trying times in semiconductor ATE market

The semiconductor industry is subject to cyclical fluctuations that are driven by factors such as technical innovations, consumer trends, and economic conditions. There is speculation in the $5 billion semiconductor automatic test equipment (ATE) industry that the market is headed for a down cycle and poised for a slowdown. Yet, there are signs of optimism.

Admittedly, 2007 was not a great year for the semiconductor ATE market, as reflected in the annual earnings of some of the big names in the industry. Teradyne's Semiconductor Test Division's revenues decreased nearly 20% over 2006 revenues, while Advantest's overall revenues slipped by almost 7%, and Verigy's revenues declined by 2.2%. Research indicates that the low demand for system-on-chip (SOC) test systems and severe pricing pressure in the flash memory market are the two major factors that led to the market slowdown during 2007.

Overall, the market is expected to continue to witness a slowdown with diminishing demand for SOC testers. The memory ATE segment, however, is expected to witness growth, as the growing use of flash memory in consumer-electronic products is expected to continue to drive the need for flash memory test systems. In fact, Verigy saw a jump in demand for its memory testers in 2007, with revenues reaching $282 million, an increase of nearly 38.2% over 2006.



Slip in revenues indicate that the semiconductor ATE market is witnessing a slowdown and what can be considered the beginning of a down cycle.

While the growth of flash memory remains almost certain, the severe pricing pressure in the flash memory market cannot be ignored. Prices have historically declined approximately 40% per year, putting pressure on ATE vendors to lower prices in turn. This will lead to increased ATE system shipments at the cost of profitability. A few participants believe that the declining flash prices will lead to increased consumption of flash memory, thereby expanding the market revenues.

One way some companies seem to be dealing with the downward trend is through the acquisition of other test companies. Verigy recently acquired Inovys, a maker of design debug, failure-analysis, and yield-acceleration equipment for semiconductor devices, and Teradyne has acquired Nextest Systems, a manufacturer of flash memory and SOC testers.

At Frost & Sullivan, we anticipate additional consolidation in the market, especially during this downward cycle, which is forecast to continue until 2011. Yet, consolidation is not the only solution for dealing with the difficult times ahead. Semiconductor manufacturing continues to concentrate in Asia, and many companies could keep an eye there during the down cycle. Asia Pacific is calling. T&MW

PCB book-to-bill

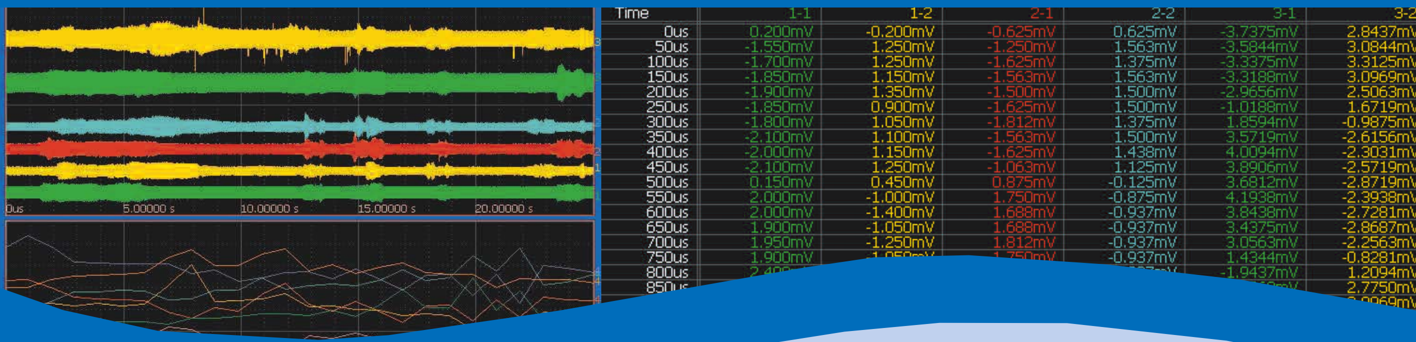
The IPC reports that for rigid and flexible printed-circuit boards (PCBs) combined, industry shipments in March 2008 increased 9.5% from March 2007, and orders booked increased 11.2% from March 2007. Year to date, combined industry shipments are up 4.6% and bookings are up 12.5%. Compared to the previous month, combined industry shipments for March 2008 are up 21.0%, bookings are up 13.0%, and the combined industry book-to-bill ratio moved up to 1.00 from 0.99. www.ipc.org.

Semiconductor equipment book-to-bill

North American-based manufacturers of semiconductor equipment posted $1.16 billion in orders in March 2008 (three-month average basis) and a book-to-bill ratio of 0.89, according to SEMI. That figure was down from 0.92 in February. "Orders reported by North American equipment manufacturers have remained at relatively constant levels over the past six months," said Dan Tracy, senior director of industry research and statistics at SEMI. "This trend is a reflection of the uncertainty in the semiconductor industry, and with current economic conditions." www.semi.org.

DisplayPort to vanquish DVI by 2011

Products with DisplayPort are hitting the market this year and will chase competing digital visual interface (DVI) technology out of the market by 2011, reports In-Stat. DisplayPort products will be limited in number in 2008, but will grow to over 600 million products shipped in 2012, the market research firm says. DisplayPort will be the first universal, digital interface between PCs and LCD monitors. DisplayPort provides 10.8-Gbps data rates, micro-packet architecture, and a scalable design that promises increased data rates in the future. In the $2995 report "DisplayPort 2008: The DVI Killer Arrives," In-Stat estimates that DisplayPort-enabled devices will grow at an annual rate of 243% from 2008 to 2012. www.in-stat.com.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50us -1.550mV 1.250mV -1.250mV 1.563mV -3.5844mV 3.0844mV
100us -1.700mV 1.250mV -1.625mV 1.375mV -3.3375mV 3.3125mV
150us -1.850mV 1.150mV -1.563mV 1.563mV -3.3188mV 3.0969mV
200us -1.900mV 1.350mV -1.500mV 1.500mV -2.9656mV 2.5063mV
250us -1.850mV 0.900mV -1.625mV 1.500mV -1.0188mV 1.6719mV
300us -1.800mV 1.050mV -1.812mV 1.375mV 1.8594mV -0.9875mV
350us -2.100mV 1.100mV -1.563mV 1.500mV 3.5719mV -2.6156mV
400us -2.000mV 1.150mV -1.625mV 1.438mV 4.0094mV -2.3031mV
450us -2.100mV 1.250mV -1.063mV 1.125mV 3.8906mV -2.5719mV
500us 0.150mV 0.450mV 0.875mV -0.125mV 3.6812mV -2.8719mV
550us 2.000mV -1.000mV 1.750mV -0.875mV 4.1938mV -2.3938mV
600us 2.000mV -1.400mV 1.688mV -0.937mV 3.8438mV -2.7281mV
650us 1.900mV -1.050mV 1.688mV -0.937mV 3.4375mV -2.8687mV
700us 1.950mV -1.250mV 1.812mV -0.937mV 3.0563mV -2.2563mV
750us 1.900mV -0.937mV 1.4344mV -0.8281mV
800us -1.9437mV 1.2094mV
2.7750mV


HIOKI 8860-50 MEMORY HiCORDER

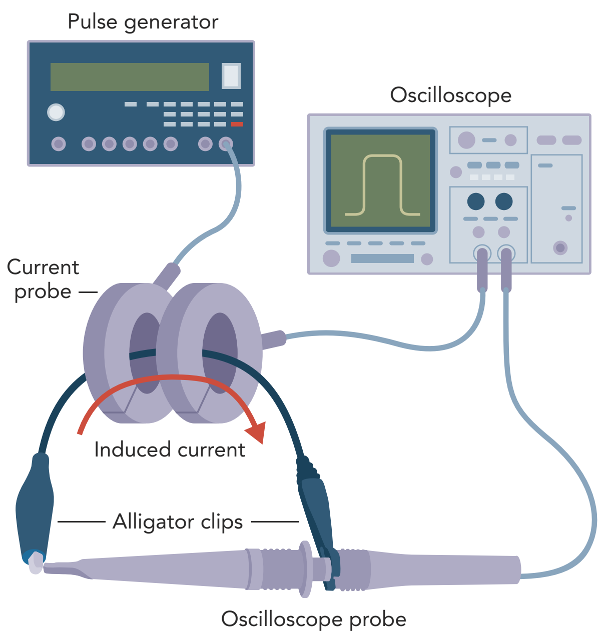
WEBCAST

Inject voltage pulses and troubleshoot

Engineers often need to test systems for immunity to voltage pulses in cables, but how do you reliably inject those pulses? In the Webcast "Inject pulses into circuits and test for EMI immunity," consultant Doug Smith explains how to use current probes to inject voltage pulses into cables. Smith, who is an expert on high-frequency measurements and electromagnetic compatibility (EMC), explains that by taking advantage of inductive coupling, you will be able to simulate conducted electromagnetic interference (EMI) in cables.

Fast pulses generate electric fields that can couple into cables and turn into current. Smith uses a pulse generator to inject up to 400 V into a cable. Because the pulses have a short duration—just tens of nanoseconds—the average power in the current probes isn't enough to damage them.

Before you can inject a voltage pulse into a system, you should measure it and the current it induces. In the Webcast, Smith shows how to induce a current into a circuit. He uses two current probes, one to induce a current in a wire (**figure**) and a second to measure the current. The wire, passing through both current probes, connects between an oscilloscope probe's tip and ground. A voltage pulse from a pulse generator produces a current in the wire. The second current probe converts the current into a corresponding voltage for the oscilloscope to display. The induced current, when injected into a system, lets you test a system's immunity to conducted EMI.



Current probes let you inject pulses into cables for conductive EMI testing.

In the Webcast, Smith also shows how to use two current probes and a spectrum analyzer to find the resonant frequency of a cable. Finding the resonant frequency of a wire is important, because the current induced by an injected voltage will peak at the cable's resonant frequency.

To see the details of how Smith sets up and performs the measurements, view the archived Webcast at www.tmworld.com/webcasts.

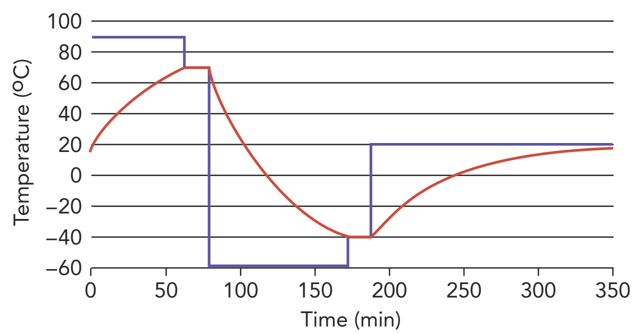
Martin Rowe, Senior Technical Editor

ENVIRONMENTAL TEST

Improve thermal cycling time

Thermal cycling tests can help you improve the reliability of electronic components, subsystems, and systems, but ensuring all areas of a product get tested at the correct temperature can be tricky. Electronic products consist of numerous materials, and each material has unique thermal characteristics. To ensure that you achieve the desired temperature at a given location, you should attach a thermocouple or other probe and monitor the temperature at the point of interest.

During your tests, keep in mind that chamber temperatures change nonlinearly and temperatures of materials used in products change exponentially. The **figure** shows material temperature (red trace) and chamber temperature (blue trace) as a function of time. Changes start out fairly linear but then roll off as the material temperature approaches the chamber temperature. After three thermal time constants of a material, it will have reached 95% of



Product temperature (red trace) rises exponentially in response to step changes in thermal-chamber temperature (blue trace).

Improve thermal cycling time *(continued)*

the chamber's temperature. It will reach 99% after five thermal time constants.

Because of the roll-off in temperature change, getting a product to reach the desired temperature at a location inside the product can take some time. To reduce cycle time, you can set a chamber's temperature above or below the desired product temperature. Doing so will keep thermal changes in the more linear portion of the cycle.

To learn more about thermal cycling and how to set chamber temperatures, you can download "Thermal cycling: Keep it linear," a paper by Mark Woolley, Jessica Greco, Wes Brown, and Dr. Jae Choi of Avaya Product Technology and Reliability Laboratory from the online version of this article at www.tmworld.com/2008_06.

Martin Rowe, Senior Technical Editor

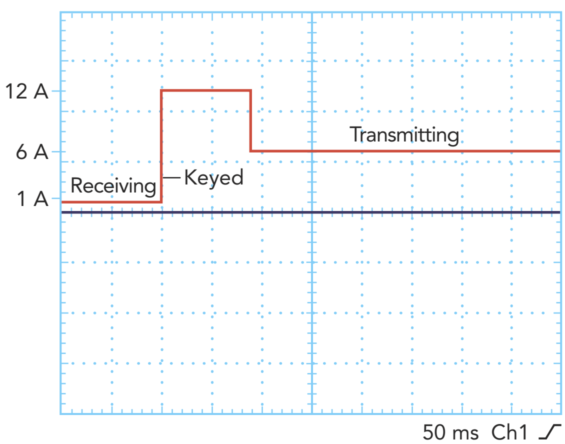
INSTRUMENTS

When power supplies don't meet specs

Randy Jones, a senior telecom specialist with the Washington State Department of Natural Resources, found that power supplies don't always meet their output specs. After some investigation, Jones uncovered the problem and a solution.

The department uses 13.8-VDC-powered VHF radio transceivers to assist firefighters with communications when they are fighting wildfires on the 12.7 million acres the department protects. Jones discovered that the radios, when transmitting, would force some of the power supplies to shut down from current overload.

"When a radio was keyed to transmit, its current consumption would jump from 1 A to 12 A," Jones said. "Although 12 A was below the maximum current rating of the power supply, the supply would shut down." The oscilloscope plot (**figure**) shows the power from the supply. When a user keyed a transmitter, the current draw jumped to 12 A before settling at 6 A.



Transceivers draw 12 A for 90 ms before dropping to 6 A while transmitting. When receiving, the transceiver draws 1 A.

A call to his power-supply supplier revealed that the manufacturer had published incorrect specifications. Jones purchased higher-rated power supplies, and the failures ceased. The manufacturer refunded the department for the cost of the original supplies.

Today, Jones doesn't buy power supplies based on manufacturer's specifications alone. He tests all new supplies before deploying them. Using an electronic load, Jones tests power supplies by setting the load to constant current. For example, one supply is tested 50% at 25 A and 50% at 35 A to ensure it operates at its rated specifications. Jones uses a logging digital multimeter to monitor the output voltage during a test.

Martin Rowe, Senior Technical Editor

INSTRUMENTS

No power interrupts, please

DEVICE UNDER TEST
Uninterruptible power supplies used in commercial and military applications. The supplies deliver up to 10 kVA at 0.7 power factor, or 7000 W.

THE CHALLENGE
Perform design verifications and production testing of uninterruptible power supplies. Verify their voltage, their frequency, and their ability to deliver the specified power to linear and nonlinear loads. Perform emissions testing. Monitor temperature of internal components. Verify the communications interface operates from battery power when expected.

THE TOOLS
- Agilent Technologies: spectrum analyzer, harmonic-distortion meter. www.tm.agilent.com.
- California Instruments: 50-Hz AC power source, 400-Hz AC power source. www.calinst.com.
- Extech Instruments: sound level meter. www.extech.com.
- Fluke: handheld DMM, power-quality analyzer. www.fluke.com.
- Stanford Research Systems: two 16-channel temperature-monitoring systems. www.thinksrs.com
- Tektronix: oscilloscope. www.tektronix.com.
- Valhalla Scientific: three-phase power and current meter. www.valhallascientific.com.

PROJECT DESCRIPTION

Uninterruptible power supplies (UPSs) deliver power to computers and communications equipment when AC mains line voltages are too low or nonexistent. The equipment must switch to battery power, and its UPS must supply uninterrupted power to the critical load until utility power is restored or until the batteries are depleted and the UPS shuts down. UPS manufacturer Falcon Electric (www.falconups.com) has been providing low-power, high-frequency online UPSs for more than 18 years.

Mike Stout, VP of engineering at Falcon, explained that engineers perform production verification by adjusting the input voltage using a variable AC power source. Using a digital multimeter (DMM), they verify that the output voltage is 122 VAC ±0.5 V under no load and the output frequency is 60 Hz ±0.1 Hz. Using trim pots, they adjust the output frequency to 60.0 Hz. Using the power analyzer, engineers verify that the total harmonic distortion (THD) of the output voltage is less than 3%.

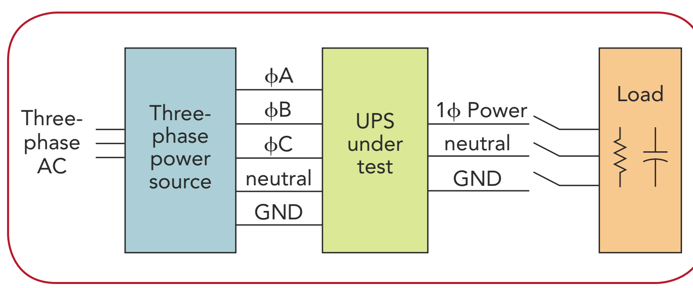
Next, engineers set the load so the UPS runs at full output power. They measure voltage and current and verify that the "full load" LED illuminates. Then, they reduce the load to the midpoint and then to the one-third power level and verify the load level display. They again measure the UPS output voltage and verify that it is within the ±3% range. They then increase the load to 25% above rated power and verify that the overload LED turns on and the UPS output overcurrent protection asserts.

Military-grade UPSs typically start drawing current from their batteries at about 60-VAC input but provide a warning at 84 VAC. Commercial-grade UPSs draw from their batteries at voltages between 80 VAC and 84 VAC. Engineers monitor the UPS output with DMMs and oscilloscopes to verify that it remains at 120 VAC ±3%.

A UPS will also switch to battery power should the AC line voltage get too high. For 220-VAC models, the UPS will typically switch from AC mains power to battery power when line voltage reaches 260 VAC. For 120-V units, a UPS must hold its output voltage to 120 VAC ±3% when the input voltage ranges from 90 VAC to 138 VAC (120 VAC –25%, +15%).

Falcon's engineers use power analyzers to verify the output current, power, and harmonics of the company's UPSs. "The highest levels of harmonic distortion typically occur at the third and fifth harmonics," said Stout. "We see very little distortion beyond the seventh harmonic." Engineers also use a spectrum analyzer to measure electromagnetic emissions.

UPSs require testing at full load, and Falcon engineers have designed their own linear and nonlinear loads for design-verification testing. The linear loads provide up to 40 kVA in 500-VA increments. Nonlinear loads simulate switching power supplies, the most common load that customers power with a UPS (see **figure**). Engineers also connect thermocouples to some components to verify that they remain within specified limits.



UPS tests require resistive and nonlinear (capacitive) loads.

LESSONS LEARNED

"When it comes to UPS power products," said Stout, "you can't over design." When the company first introduced its online UPS, the design was so robust that the engineers were able to increase the power output without increasing heat sink sizes in many cases. "A good solid design is essential as there is no money in returns," Stout said.

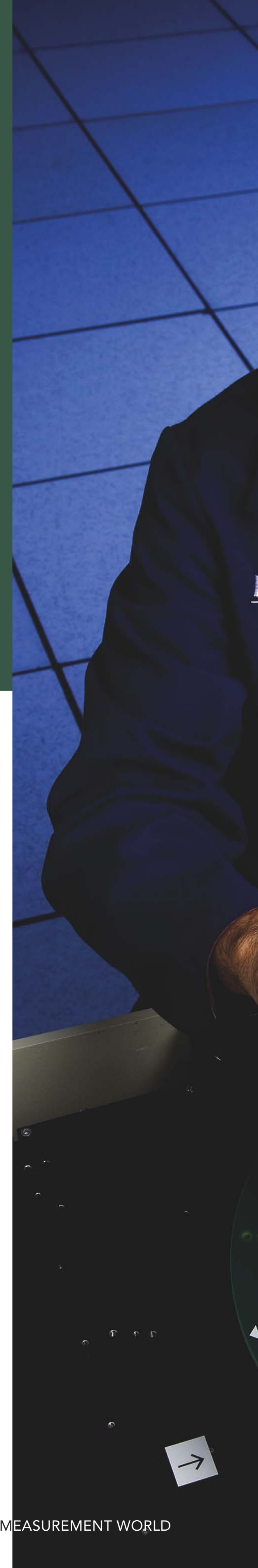
Martin Rowe, Senior Technical Editor

ON THE ROAD

SEMICONDUCTOR TEST

FROM TAPE-OUT to YIELD

BY RICK NELSON, EDITOR IN CHIEF



San Jose, CA—Nanometer semiconductor devices present significant validation, characterization, and analysis challenges as designs move from tape-out to high-volume production. To help chip makers get such devices to market quickly, Presto Engineering deploys a variety of test and analysis equipment and augments that equipment with expertise in packaging, thermal control, sample prep, and—most critically for deep-submicron devices with increasing numbers of metallization layers—backside analysis.

The company's goal is to complement customers' in-house product-engineering, test, and failure-analysis capabilities when chip makers find their expertise in one or more of these areas is scarce, or where unusual test requirements would otherwise dictate the purchase of equipment that would be too costly to bring in house. Deficiencies that Presto can address might include lack of the equipment and trained personnel necessary to handle backside in-circuit analysis (photon emission measurement, laser stimulation/analysis, laser voltage probing, and backside focused ion-beam [FIB] probing) in combination with automated-test-equipment (ATE) operation and programming.

Presto Engineering occupies the 10,000-ft^2 test floor formerly owned by Cypress Semiconductor, dedicating three-shift operation to provide test, fault-isolation, and failure-analysis services, according to Michel Villemain, founder and CEO. The goal, he said, is to complement, not displace, traditional test houses and analytical labs (**Figure 1**).

"Test houses," Villemain said, "are on one side and primarily focus on capturing volume business. And you have the analytical labs on the other side, which have no notion

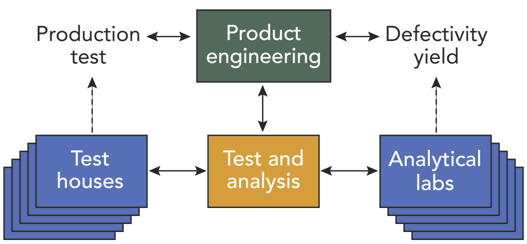


FIGURE 1. Able to provide test and analysis services, Presto Engineering works with product engineering, test houses, and analytical labs.

PRESTO ENGINEERING COMBINES TEST, BACKSIDE ANALYSIS, PACKAGING, AND THERMAL-CONTROL CAPABILITIES TO SPEED CHIPS TO MARKET.

GARY LAUFMAN

of the product itself—they don't have testers, and they don't have access to design information, so there is a gap. And what we are planning on is filling that gap." To do that, the company deploys its equipment and expertise to address the product bring-up time between tape-out and high-volume production (**Figure 2**).

Villemain is well positioned to tailor the available equipment to test and analysis applications, having served most recently as marketing VP for the circuit-edit and mask-repair division at FEI. He was also GM of the CD-SEM business unit at KLA-Tencor, and he began his career in the semiconductor test industry with Schlumberger (which later became NPTest, which in turn was bought by Credence Systems), where he worked in the company's ATE and probe-systems divisions.

Villemain, who graduated from Ecole Polytechnique in Paris and holds a PhD in computer science from Orsay University, is complemented at Presto by co-founder and engineering VP Frank Sauk, who has more than 25 years of experience in the semiconductor test and failure-analysis industry. Sauk, who holds MS and BS degrees in electrical engineering and computer science from MIT,

◀ **Frank Sauk, Presto Engineering's co-founder and engineering VP, works with Presto's Allegheny prototype for temperature and high-power SIL characterization.**

most recently served as director of diagnostic services and member of the technical staff at Credence Systems. He was also a founding member of the SABER (Schlumberger Advanced Business Engineering Resources) organization within Schlumberger, where he was responsible for failure-analysis services.

Scan test's role in characterization

Villemain said Presto employs a variety of fault-isolation and failure-analysis techniques, including mechanical probing for electrical measurements as well as laser-based techniques (to localize faults to specific vias) and emission-based techniques (for examining transistor performance). The company complements those tools with scan-based localization to pinpoint defective gates. "I'm a big believer in scan test," he said, "and we are trying to push and expand the coverage of scan test for validation and characterization and analysis as much as we can."

Cost is one factor that makes scan test attractive, Villemain said, presenting a graph (**Figure 3**) of per-pin test costs and total tester costs over the last 23 years. Today, a dedicated scan tester costs between $200,000 and $400,000, compared with almost $8 million for a 400-MHz functional tester in 1995. On a per-pin basis, 512-pin scan tester costs can be as low as $500 per pin, compared with more than $15,000 per pin for a 1990 Schlumberger ITS 9000FX with 192 pins. Going forward, Villemain said, "The whole concept of DFT [design for test] and investing up front to reduce cost downstream is going to be very pervasive. The cost equation for test has been completely reset."

Villemain said he realizes that a customer may not want to use a scan-focused tester for high-volume production. He acknowledged that manufacturers want to avoid dual-platform production test solutions because of the correlation nightmares that multiple-platform approaches might entail. Nevertheless, he recommends what he calls a dual-test-platform approach for validation and characterization before chips reach the high-volume production stage.

This approach, as he explained it, uses a scan tester for validating all circuitry accessible via scan or built-in self-test (BIST). I/O characterization can then take place on the customer's target production tester. As to what that production tester should be, he said, "Presto is tester-agnostic."

The dual-platform approach, he said, can offer significant savings, especially if Presto's customer can supply standard test interface language (STIL) or WGL files, enabling Presto engineers to bring up the scan-test program in a day or less. Describing a typical bring-up scenario, Villemain said that five weeks of characterization on a functional tester can cost $60,000. Alternatively, the dual-platform approach requires four weeks on a scan tester for $16,000, in parallel with two weeks on the functional tester, costing $24,000, for a total characterization cost of $40,000, resulting in a $20,000 savings.

Presto Engineering founder and CEO Michel Villemain said that manufacturers have shied away from backside analysis because of its complexity, but he adds that the technique is becoming indispensable at the 65-nm process node.

GARY LAUFMAN

When factoring all project functions, ranging from load-board development to the porting of BIST vectors to production ATE, the dual-platform approach, he said, can yield a total project cost of only $167,000 with a 17-week turnaround vs. $242,000 with a 21-week turnaround for a functional-ATE-only approach.

The need for backside analysis

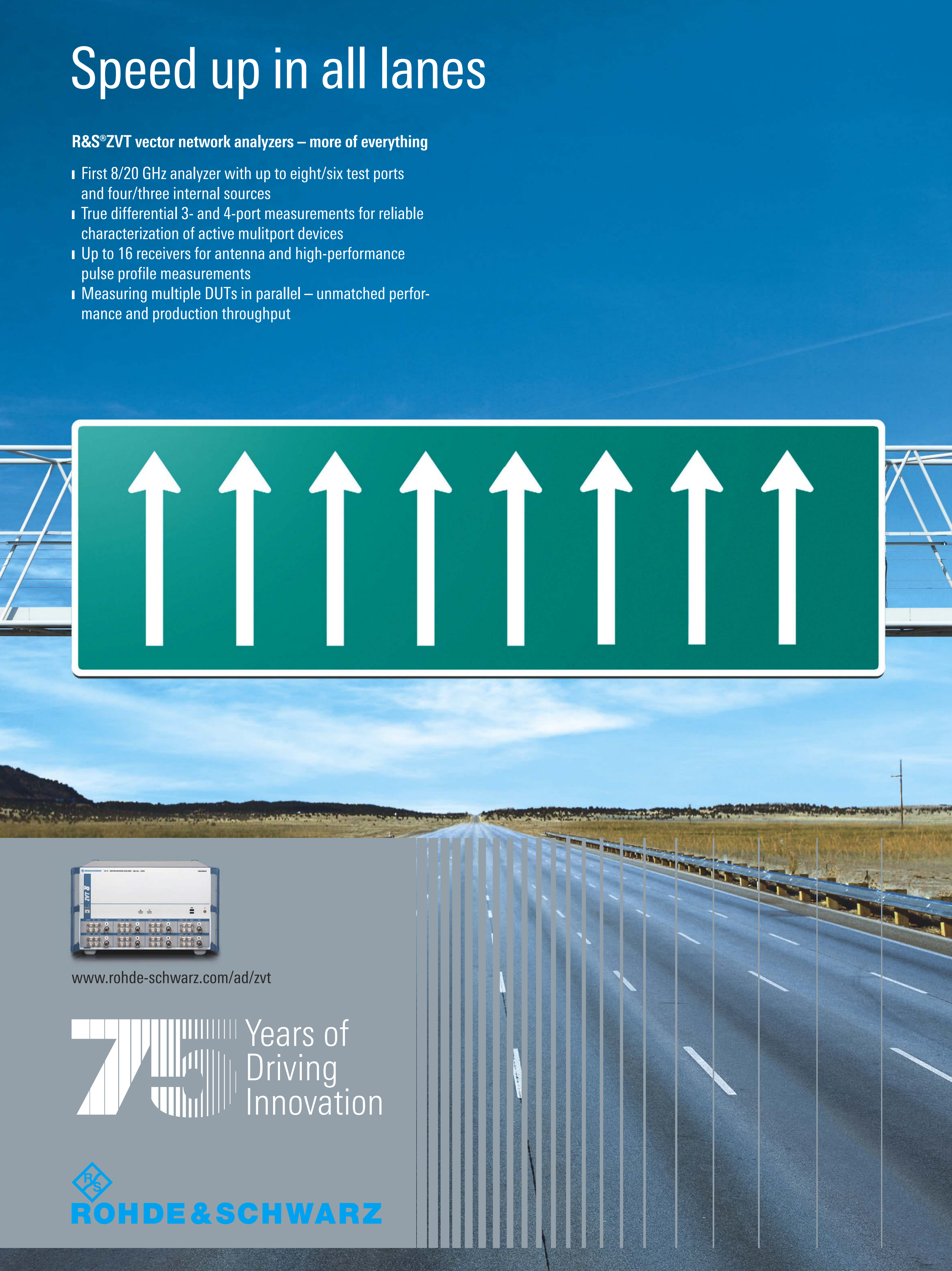
Villemain said he expects the need for his company's services to expand as process geometries shrink. At the 130-nm node, he said, manufacturers supported 46 captive product-analysis labs in North America, while at the 65-nm node, the number is only 12—but not because chips are sailing into production without any re-spins. In fact, Sauk estimated that fewer than 40% of IC designs go to production with first silicon.

Villemain sees three reasons for the reduction in the number of captive test houses:

- the cost of 65-nm-capable equipment,
- the necessary transition from front-side to backside analysis, which requires hard-to-develop and hard-to-retain expertise, and
- the complex requirement of combining test equipment with analysis equipment to provide stimulus during the analysis process.

Companies that rarely need such equipment and expertise, he said, cannot justify the huge investment necessary to bring the required analytical capabilities for new process nodes in house.

Villemain and Sauk both emphasized that backside analysis is definitely necessary because the increasing number of metal layers is preventing front-side analysis. "The traditional toolset used to isolate faults—such as metal-centric (front-side e-beam) probing and FIB circuit edit—become very difficult to use when you have more than three or four metal layers and buried elements become harder to access," said Sauk. But, added Villemain,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"There is a perception gap, causing manufacturers to avoid backside analysis for fear it's too complex and won't work."

Villemain acknowledged that backside analysis tools are complex and require much practice to use effectively. In addition, the techniques can be conceptually difficult to understand. "E-beam was difficult enough, but it was fairly simple to explain—you have electrons in and secondary electrons out," he said. "But how do you explain all these laser-related techniques? It's very arcane."

Complicating the matter, he said, is the fact that "backside measurements are proxy measurements…your transistor switches and emits a photon once in a while. You need mentally to bridge what you see on your photon-emission system's screen to what you need to understand about your product. Now, e-beam is a proxy measurement, too, but it's a simple proxy. The other techniques are more complex and require a lot of interpretation. So, there is a knowledge gap."

But despite the complexity of backside analysis, he said, "I've been providing these tools for 10 years now, and I've seen them in operation in a lot of labs. Backside analysis does require different approaches, but it does work. It's a perception gap that is really an issue that needs to be bridged."

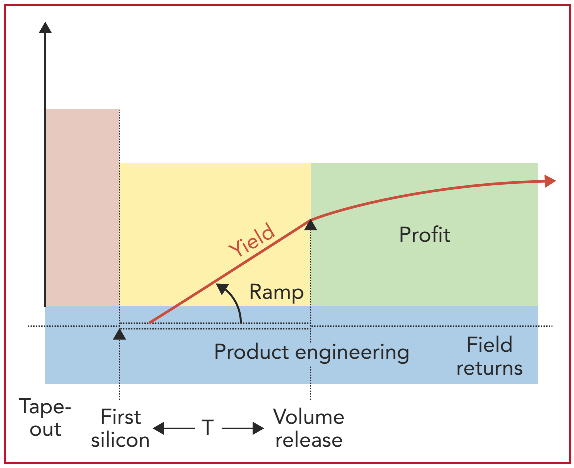

FIGURE 2. Capabilities that Presto Engineering offers include PrestoConnect, which operates from tape-out to first silicon, and PrestoPE, which operates during ramp-up to profitable yield.

Random and soft defects

Villemain cited other issues that complicate test and analysis, including the transition from predominantly random defects to predominantly systematic ones. Addressing systematic defects requires close links between design, test, and analysis. In addition, he said, many defects in advanced processes are soft—occurring only at certain voltages or temperatures, for example. If a soft error occurs only at –40°C, he said, you need to be able to duplicate that condition during backside analysis.

Sauk elaborated on the difficulty that can occur during backside analysis. You need to remove any existing fans, lids, or heat sinks to provide visibility into the

silicon, yet you need to retain a way to control the temperature. For that, Presto uses heat spreaders that provide temperature control while enabling visibility into the device under test.

For visibility, Sauk said, "Solid immersion lenses [SIL] are popular for 65 and 45 nm, but they change the dynamic of what you are analyzing, because the lens has to touch the silicon." Diamond is an ideal heat spreader, but until recently it could not be used in conjunction with SILs due to the requirement for direct contact between lens and silicon, he said, but added, "We've gone back to an older technique using copper to touch part of the silicon and expose the remaining part of it. We provide a way to move the insert that touches the die so you choose what part of the die you'll cover and what part you'll measure. This approach works fine up to 75 W." For higher power up to 300 W, he said, Presto still uses diamond spreaders with liquid-immersion or air-gap lenses.

For applications that can benefit from the use of a solid-immersion lens at high power, the company has developed a device called Allegheny (pictured on the cover and on p. 27) that combines the two techniques. It includes a hole in the diamond portion to provide compatibility with the SIL; the diamond window can move in all directions across the die. "The fact we can combine the SIL with the diamond means we can support local or global analysis with the same cooling hardware. A prototype of this new heat spreader is currently in beta testing, with production release scheduled for later this year," Sauk said.

He added that soft errors caused by cosmic rays and alpha particles continue to be a primary concern as well for memory and logic designs targeting 65 nm and smaller processes. Presto, Sauk said, has recently established a collaborative sales and service relationship with iRoC Technologies, allowing customers in North America access to the SERTEST soft error rate testing services.

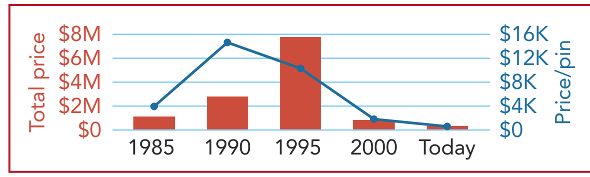

FIGURE 3. Presto Engineering deploys a dedicated scan tester, which delivers 512-pin performance at approximately $500 per pin today, demonstrating how tester prices have fallen from a high per-pin cost of $15,000 for a Schlumberger ITS 9000FX in 1990 and a high total cost of $8 million for a high-end 400-MHz machine in 1995.

Equipment line-up

To help take chips from tape-out to high-volume production, Presto deploys an Ocelot ATE system for scan test. It has on hand a SEMICAPS SOM 4000 scanning-optical microscope, which combines a photo-emission microscope and laser-scanning microscope for fault


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isolation. A Schlumberger IDS 10000plus e-beam system and mechanical probers support electrical failure analysis.

In addition, Presto partners with Nanolab Technologies, which is located near Presto's facility, to make available a Sonoscan C-SAM scanning-acoustic microscope, an FEI NanoSEM 630 scanning-electron microscope (SEM), an FEI V-600 FIB system, a JEOL 3010 transmission-electron microscope, and an 8-in.-wafer-capable FEI 855 dual-beam FIB/SEM system. Other capabilities include sample de-cap and de-processing, backside sample preparation, deep ultraviolet microscopy, and real-time x-ray.

The company's PrestoConnect service extends from tape-out to first silicon, while PrestoPE (the PE stands for "product engineering") extends from first silicon to high-volume production. Services include packaging, docking assemblies, thermal interfaces, load-board development, cooling design, validation, characterization, test engineering, electrostatic discharge/latch-up troubleshooting, environmental screening, debug, fault isolation, failure analysis, and root-cause analysis.

The initial point of engagement with customers is packaging, Sauk said. Presto provides analysis-ready packages—including backside-ready packages for wire-bonded devices—that work with standard load boards. "When we sit down with customers, we go through a process in which we determine pad count, pad pitch, die size, and wire length."

Presto now offers 680- and 532-ball ball-grid arrays (BGAs) and 256-pin pin-grid arrays (PGAs); the company will design and build new packages when necessary. The packaging process—including die-attach and wire-bonding, encapsulation and ball-attach, and sample preparation (including thinning and polishing)—takes about a week, Sauk said, with yields of 90%. For analysis of field returns, the repackaging process (including parallel polishing down to wire-bond balls, die-extraction, die-attach, wire-bonding, encapsulation, ball-attach, and sample prep) requires a turnaround time of about two weeks and offers a yield of 60% to 80%.

With access to the backside, Sauk said, "we can do time-resolved emission and laser scanning, and even e-beam is making a resurgence." E-beam techniques, he said, derive some timing and voltage information not available with other approaches. "Each of these techniques has strengths," Sauk said, "but each has gaps as well."

The ability to understand where the gaps lie and compensate for them will be key to getting next-generation chips to market. As process geometries continue to shrink and the number of metallization layers increases, effective failure analysis will become increasingly important. But on a final note, Villemain suggested—facetiously—that failure analysis might disappear as a discipline. "My marketing team tells me 'failure analysis' has a bad connotation. What we provide at Presto is 'design success analysis.'" T&MW

THE ANALOG SIGNAL PATH IS FULL OF TRADEOFFS AND DECISIONS THAT AFFECT OVERALL PERFORMANCE.

Design TRADEOFFS in data acquisition

BY MARTIN ROWE, SENIOR TECHNICAL EDITOR

The analog acquisition section is the heart of any data-acquisition system. Microprocessors, digital-signal processors, memory, firmware, software drivers, operating systems, and software applications may form the brains of a system, but they're only as good as the analog circuits. To build a system that has the necessary speed, resolution, and accuracy for a given application, you need to find the right combination of analog data converters, op amps, multiplexers, and voltage references.

Figure 1 shows the basic analog signal path through the analog-to-digital converter (ADC). Every data-acquisition system uses some form of this basic configuration. The choice you make for each component will affect the options available for the other components.

The analog signal path begins at the input connectors. Most data-acquisition systems have some form of circuit protection before the analog circuits. Components such as fuses or clamping diodes limit the voltage or current that enters a system, thus protecting its components from harm.

Data-acquisition systems seldom have a single measurement channel. Digital multimeters (DMMs) typically have one channel, but you can combine a DMM with relays to increase channel count. Data-acquisition systems, whether plug-in boards, USB modules, or stand-alone systems, may have a dedicated ADC per channel, or they may have a single ADC with a multiplexer (mux) connected to multiple channels. The use of a dedicated ADC for each channel lets the system simultaneously sample on all channels.

Following the mux (if the system has one), a programmable-gain amplifier (PGA) amplifies or attenuates the input voltage from a sensor or other signal source to best match the ADC's input voltage range. Some systems may include a second op amp that adds a DC offset voltage to the input signal. The offset voltage shifts the signal so it's centered in the input range of the ADC. The ADC's

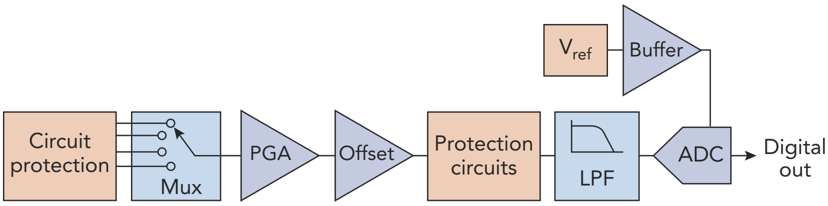

FIGURE 1. Analog channels consist of components such as a programmable-gain amplifier (PGA), an offset amplifier, and a low-pass filter (LPF). Courtesy of National Instruments.

input voltage range, therefore, has a major influence on your choice of PGA.

You may also use additional clamp circuits to protect the ADC. Just prior to the ADC, most system designers add a low-pass anti-aliasing filter. This filter limits the signal path's bandwidth and is the last chance to minimize aliasing before the ADC digitizes the signal.

To successfully digitize analog signals, ADCs need a reference voltage, V_{ref}. Some ADCs have an internal reference while others use an external reference source.

"We prefer an external voltage reference," said Kevin Cawley, senior principal engineer at Keithley Instruments. "We believe that external voltage references are more stable than internal ones."

Alex Ivchenko, engineering manager at United Electronic Industries (UEI), went a step further. "If you have an external reference, you can adjust the gain of the input path by controlling the ADC reference voltage," he said. "If your input voltage is too high, you need to provide a higher V_{ref}."

An ADC's digital output can be in either serial or parallel form. The serial bus offers improved analog performance because fewer lines will change state at a given time, which minimizes bouncing on the power and ground lines and reduces overall system noise. But because serial interfaces run at higher clock speeds than parallel buses for the same number of bits, you must carefully route signals to keep the noise down.

Choosing an ADC

The choice of ADC leads to numerous design tradeoffs that you must consider. Most ADCs used in data-acquisition systems use successive-approximation register (SAR) or sigma-delta (ΣΔ) architectures. In general, SAR devices yield higher speeds than ΣΔ ADCs, but ΣΔ architectures produce finer resolution. If you need better than 18-bit resolution, you'll need a ΣΔ converter.

The sample rate and power-supply voltages of the ADC will determine the type of support circuits you can use. Consider, for example, the supply voltage. Most of today's ADCs are made from a CMOS process rather than from a bipolar process. CMOS devices operate with considerably less power than bipolar devices. They can also operate with lower power-supply voltage rails. Where bipolar devices may need ±12-V or ±15-V rails, CMOS devices run from unipolar power supplies of 5 V, 4 V, 3.3 V, 2.5 V, and even 1.8 V.

Although the low voltages reduce power consumption, they also compress an ADC's dynamic range. An ADC that operates at ±12 V has six times the dynamic range of a 0–4 V device. Thus, an equal amount of noise will impact the ±12-V system far less than on a 4-V system. You must, therefore, keep the noise entering an ADC to less than 1 least-significant bit (LSB). You need an op amp with a noise level consistent with the dynamic range of an LSB in front of the ADC. That means you'll need lower noise for a 24-bit ADC than you will for a 16-bit ADC.

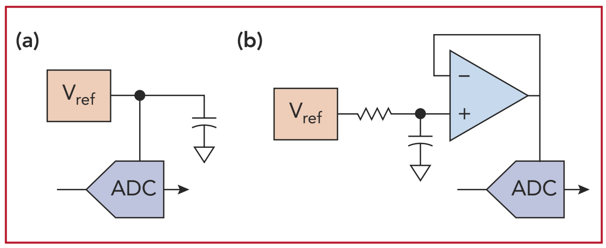

FIGURE 2. Voltage references often need (a) a bypass capacitor or (b) a capacitor with a buffer amplifier.

To get the best dynamic range, you should push the high-level signals as far into the analog channel as possible, according to Cawley. He noted that Keithley's DMMs provide the best accuracy at the 10-V range where they need neither amplification nor attenuation of the incoming signal.

Designers push back

Because of the better dynamic range that higher-voltage rails offer, many designers of industrial data-acquisition systems demand such rails for their op amps and data converters. As a result, ADC manufacturers have developed CMOS data converters that operate at ±16-V power rails. These devices can handle sensor inputs up to ±15 V, noted Chris Hyde, senior field applications engineer at Analog Devices.

Another compensation for the low dynamic range is to digitize your sensor signal as early as possible. "High-speed ADCs have come down in price to the point where oversampling makes sense," said UEI's Ivchenko.

With oversampling, you can use digital filtering to reduce noise. The more you oversample and filter, the better the noise immunity, but the slower the system. Ivchenko pointed out that oversampling by 2^{2n} and using a digital averaging filter will improve noise performance. The **table** lists how much oversampling is needed to improve noise performance by a given number of bits.

Following the ADC, Ivchenko applies a "brick wall" (120 dB/octave) digital finite impulse response (FIR) filter to reduce noise and extract the spectrum of interest. Then, he decimates a portion of the data or he applies a moving average to make the sample rate acceptable for the application.

Low-voltage ADCs and op amps need sufficient current to supply and keep signals stable during data conversion. "Designers often pick op amps and voltage references that don't have enough drive," said Hyde. "A voltage reference may need to both source and sink current." An ADC may have a dynamic input impedance and may need a low-impedance signal source with sufficient coupling to maintain the reference voltage level.

"SAR converters need a very low output impedance source to keep the input signal from varying during conversion," said Luis Orozco, analog design engineer at National Instruments. "Because SAR ADCs usually present a highly dynamic load to their power supply, we carefully bypass all devices." He noted that matching the correct op amp to an ADC is critical.

(continued)

The amount of over-sampling needed to improve noise performance by a given number of bits

Noise improvement (bits, *n*)	Amount of oversampling needed (2^{2n})
1	4
2	16
3	64
4	256

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"An op amp with the required performance to achieve the advertised ADC specs may consume several times the current that an ADC uses," Orozco said. The reference input on ADCs behaves similarly to the signal input. Low-power devices such as voltage references may need capacitors or buffers to maintain their output at a stable level as the ADC samples its reference.

"Not only that," added Ivchenko, "but you should use low equivalent-series resistance [ESR] bypass capacitors. Use X7R ceramics rather than tantalum capacitors whenever possible. A capacitor must charge or discharge quickly enough to feed sufficient peak current to an ADC during a conversion cycle." A high ESR will increase a capacitor's charge and discharge time.

Figure 2 shows both ways to provide ample current. In Figure 2a, a capacitor stores energy and supplies it when the ADC needs additional current to keep the reference voltage stable. A 22-μF capacitor

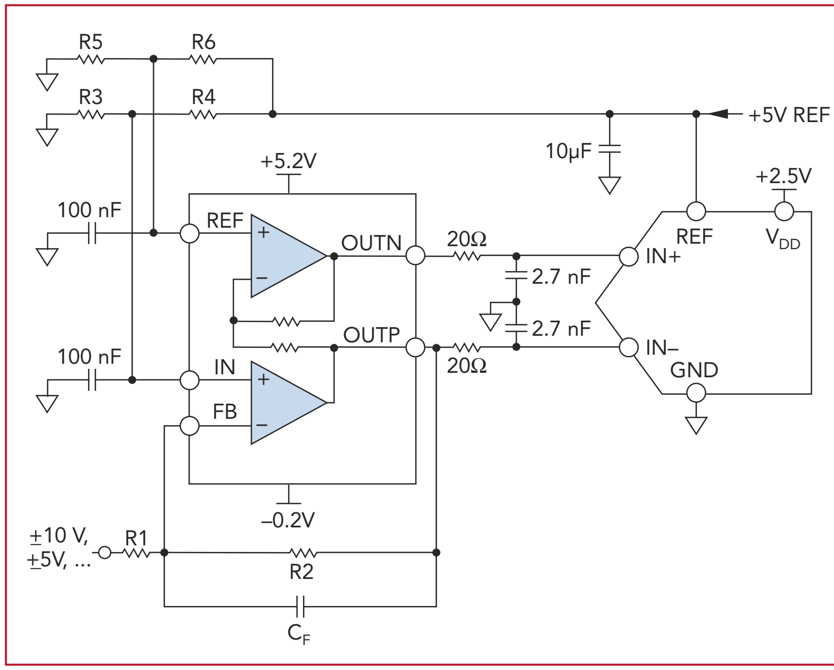

FIGURE 3. A single-ended-to-differential converter circuit lets you digitize differential signals. Courtesy of Analog Devices.


"click"
"click"
"click"

is usually sufficient, but check your ADC's data sheet to be sure. In Figure 2b, an op amp buffers the voltage reference from the ADC. The op amp provides the voltage reference with a high-impedance input while its low-impedance output provides enough current for the ADC. While the op-amp solution is more elegant, it adds an offset voltage to V_{ref}, it adds noise to the system, it increases power consumption, and it is more expensive.

Differential inputs

To improve dynamic range and noise rejection, you should use differential inputs in your data-acquisition system. With differential (as opposed to single-ended) inputs, any signals common to both signal lines will be negated to the best of the ability of the common-mode rejection (CMR) amplifier or the ADC. If your sensor's output is single ended, you can use a single-ended-to-differential converter driver circuit (**Figure 3**). You can design your data-acquisition system to use single-ended or differential inputs.

Many data-acquisition systems have a mux that adds channels. Resistance and capacitance in a mux can affect signal integrity. For example, charge injection from a mux can turn DC signals into AC signals. The on-resistance (R_{on}) combines with parasitic capacitance to form a low-pass filter, which has an RC time constant. **Figure 4** shows what happens if the time constant is too long relative to sampling time.

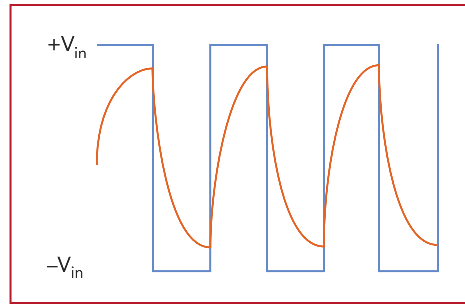

FIGURE 4. Charge injection, on-resistance, and parasitic capacitance can cause leakage across adjacent channels in multiplexed systems.

You can easily test your system for this error. Connect two adjacent channels in a multiplexed data-acquisition system (such as channels 0 and 1) to DC voltages near the system's input limits, say +10 V and –10 V. Next, alternate samples between the two input channels. Start with several samples on each channel and gradually move to one sample per channel before switching channels.

If the time constant is fast compared to the sample rate, then you should see a square wave at one-half the sample rate. But if the time constant is too long, you'll get what resembles a triangle wave because of charge injection between the channels.

"R_{on} should be no more than a few ohms," said Hyde of Analog Devices. "On-resistances of a few hundred ohms are too much for many of today's data-acquisition applications." National Instruments'

Orozco contends that a few hundred ohms isn't too much because of the high input resistance of the upstream op amp.

Hyde also pointed out that a mux's on-resistance can change based on the amplitude of the system's input signal. If you change channels from one voltage rail to the other, you need to know the RC time constant of the channel. While R_{on} changes with voltage, channel capacitance causes an impedance change with frequency. These impedances work against the capacitance to form a variable low-pass filter and cause distortion.

"The channel must settle within the accuracy limits of the ADC to prevent charge-induced errors," said Hyde, and he added that newer muxes have lower capacitance than older models.

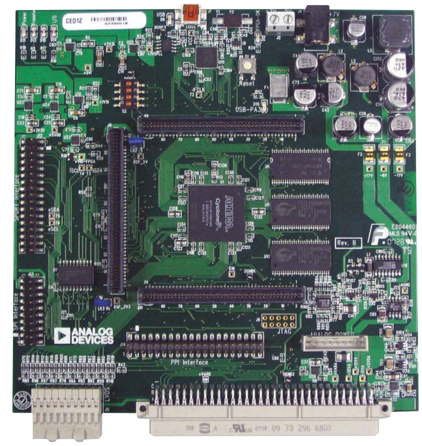

FIGURE 5. Reference design boards provide support circuits and communications that let you test an ADC.

Courtesy of Analog Devices.

Technical data

When designing a data-acquisition system, you will certainly rely on the data sheets for the ADC, op amps, and voltage references. Component makers also provide another valuable resource—the reference design board—for their parts (**Figure 5**). Often, you can purchase a reference design board to evaluate parts before designing them into a system.

Data sheets also provide design and layout information, but as Keithley's Cawley found out, information on data sheets and reference design boards may differ. When designing a 500-ksamples/s, 18-bit data-acquisition system, Cawley relied on the design information in a data sheet, only to find that the ADC produced between 3 and 7 LSBs of noise (5 μV/LSB). "When I switched to the layout recommended in the reference design, the noise dropped to within 1 LSB" he said. "The reference design used four layers of ground under the quad-flat-pack (QFP) device. Nine vias connected the ground planes, but the data sheet used a trace from the ADC to a bypass cap instead of using a ground plane."

Analog IC manufacturers offer extensive technical information on designing with ADC. You can find application notes, data sheets, online seminars, technical papers, and simulation software available at no cost. The online version of this article contains links to many of these resources, www.tmworld.com/2008_06. T&MW

PROTOCOL STACK TESTING *for* LTE

EFFECTIVE TEST STRATEGIES CAN HELP TRANSFORM UMTS INTO A CELLULAR WIDEBAND SYSTEM.

BY CHRISTINA GEßNER, ROHDE & SCHWARZ

Producers of mobile phones and mobile infrastructure are working on the next big step in the development of the universal mobile telecommunications system (UMTS): UMTS long term evolution (LTE). The new standard will ensure that UMTS remains competitive while giving users enhanced mobile Internet access. The first commercial LTE networks could be in place by 2010, and LTE standardization is progressing as part of Release 8 from the 3rd Generation Partnership Project (3GPP). Manufacturers, therefore, will soon need suitable test capability to verify their LTE products.

LTE networks must provide downlink data rates of higher than 100 Mbps and uplink rates of higher than 50 Mbps. They must also significantly reduce the latency times for packet transmissions so users won't experience unacceptable delays. To achieve these goals, the 3GPP is defining new air-interface transmission methods and is also revamping the protocol and network architecture of UMTS.

Where UMTS used wideband code-division multiple access (WCDMA) for transmitting signals, the LTE downlink uses orthogonal frequency-division multiple access (OFDMA), which is particularly robust when handling the varying propagation conditions seen in mobile radio. The LTE uplink will employ single-carrier frequency-division multiple access (SC-FDMA), which can be considered a precoded OFDMA.

Another significant feature of LTE is its high bandwidth—up to 20 MHz. Because the usable bandwidth is scalable, LTE can also operate in the existing 5-MHz UMTS frequency bands, or in even smaller bands. Developers of LTE base stations and wireless devices must also account for a very short latency time; LTE has a transmission time interval of only 1 ms between data packets.

LTE systems can also employ multiple-input multiple-output (MIMO) antenna systems. In one MIMO technique, multiple antennas can transmit the same data stream to improve data-transmission reliability, resulting in diversity gain. In another, the different antennas can transmit different data streams simultaneously to increase throughput; this method is called spatial multiplexing and results in multiplexing gain. Spatial multiplexing is necessary to achieve the greater

than 100-Mbps data rates in the downlink direction.

An LTE base station can have up to four transmit antennas, and an LTE wireless device will have up to four receive antennas. Initial implementations will probably consist of 2x2 systems—that is, two antennas on the transmit end and two on the receive end.

The protocol architecture of LTE

The 3GPP is completely reworking the network and protocol architecture of UMTS so LTE can support high data rates and short latency times. LTE is a purely packet-oriented technology developed in accordance with the 3GPP's System Architecture Evolution (SAE) effort. LTE uses a minimal network architecture to reduce latency time. **Figure 1** provides an overview of the LTE network elements and their interfaces. The LTE base station, or eNodeB (eNB), initiates connections on the air interface. It also assigns air-interface resources and performs scheduling.

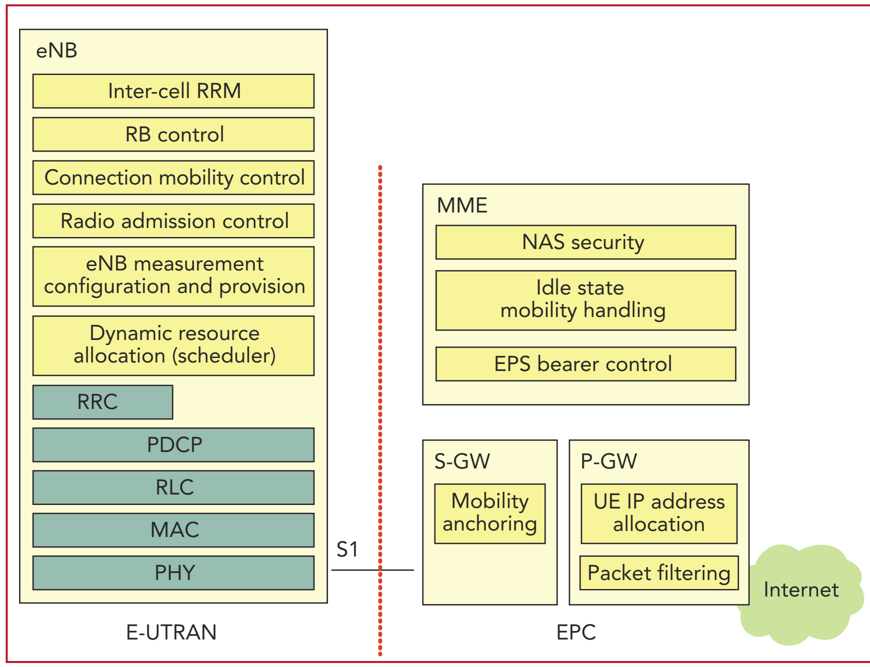

FIGURE 1. In an LTE network, a base station (eNB) connects to a core network via the S1 interface. Multiple eNBs connect to each other via the X2 interface (not shown).

Each LTE base station connects to the core network through the 3GPP-defined S1 interface. The base stations themselves are interconnected via the X2 interface so they can initiate and complete actions such as handovers. As a result, the radio network controller (RNC) previously used in UMTS is no longer needed, which significantly reduces the number of internal interfaces in the network. The eNB basically assumes the functions previously handled by the RNC.

Figure 2 shows the protocol architecture for the user plane and control plane. The layer-1 and layer-2 protocols of the air interface terminate in the wireless device and in the eNB. The layer-2 protocols include the medium access control (MAC) protocol, the radio link control (RLC) protocol, and the packet data convergence protocol (PDCP). The layer-3 radio resource control (RRC) protocol also terminates in both the wireless device and the base station. The protocols of the non-access stratum (NAS) in the control plane terminate in the wireless device and in the mobility management entity (MME) of the core network.

Many of the procedures used for UMTS have been simplified for LTE. For example, LTE employs the shared-channel principle, which provides multiple users with dynamic access to the air interface. In contrast to the conventional circuit-switched operation, the packet-oriented LTE network does not assign resources to a user for the entire duration of a connection. Instead, the base station gives the user a resource on the shared channel only when a data packet is to be transmitted. During transmission pauses, the resource can be assigned to other subscribers. The dedicated channels used in GSM and UMTS are thus no longer needed, greatly simplifying the LTE protocol architecture and ensuring efficient use of the resources on the air interface.

The addition of procedures for link adaptation further improves the performance of the

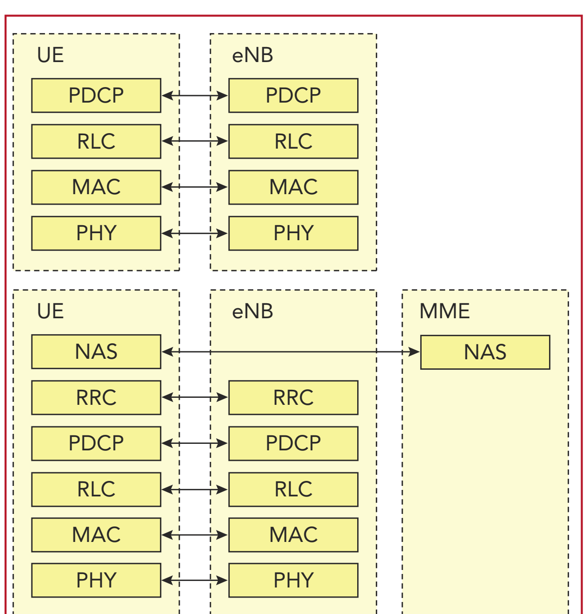

FIGURE 2. In the LTE protocol architecture for user plane (top) and control plane (bottom), layer-1 and layer-2 air-interface protocols terminate in the wireless device and in the eNB. The layer-2 protocols include the MAC protocol, the RLC protocol, and the PDCP. The layer-3 RRC protocol also terminates in both the wireless device and the base station. The protocols of the NAS in the control plane terminate in the wireless device and in the MME of the core network.

shared channels. With link adaptation, the base station selects the optimum modulation and coding scheme based on the connection quality. The base station also makes frequency-dependent scheduling decisions, such as whether a user would have better connection quality in a specific range of bandwidths.

The scheduling mechanism is therefore complex and if not properly implanted can significantly degrade the performance of the LTE system. The stringent timing requirements are of particular importance because the base station makes a scheduling decision every millisecond.

LTE differs from UMTS in dispensing with the compressed mode of WCDMA, which allows a wireless device to take measurements on other frequencies or radio technologies to optimize call quality and to facilitate handovers. For this purpose, data transmission is compressed so that the wireless device can find gaps for performing measurements. This method is relatively complex to implement. Because LTE doesn't use compressed WCDMA, the base station is responsible for providing individual subscribers with the necessary pauses for these measurements.

An important aspect, particularly from the point of view of network operators, is the integration of LTE into established mobile radio networks. In addition to GSM/GPRS and the existing UMTS networks, these include networks that are based on WiMAX and CDMA2000. To ensure the successful handover of calls from LTE networks to ones based on other technologies, the 3GPP specifies suitable handover mechanisms.

Protocol tests for LTE devices

During the early stages of development of LTE-capable chipsets and wireless devices, engineers should perform protocol tests as well as a functional test to ensure that the functioning of the protocols on the air interface complies with the 3GPP LTE specifications. Engineers should also address performance aspects, such as whether the product can handle the high-data-rate requirements of LTE.

Depending on the degree of integration, you can use various approaches for performing protocol tests. Several test-equipment manufacturers offer test instruments that include software-based LTE protocol testers. If a layer-1 implementation is not yet available, or integration has not yet taken place, you can use this software to perform a virtual test of the protocol software. In the R&S CMW500 for LTE, for example, the test software emulates the behavior of the protocols on the network end. Develop-

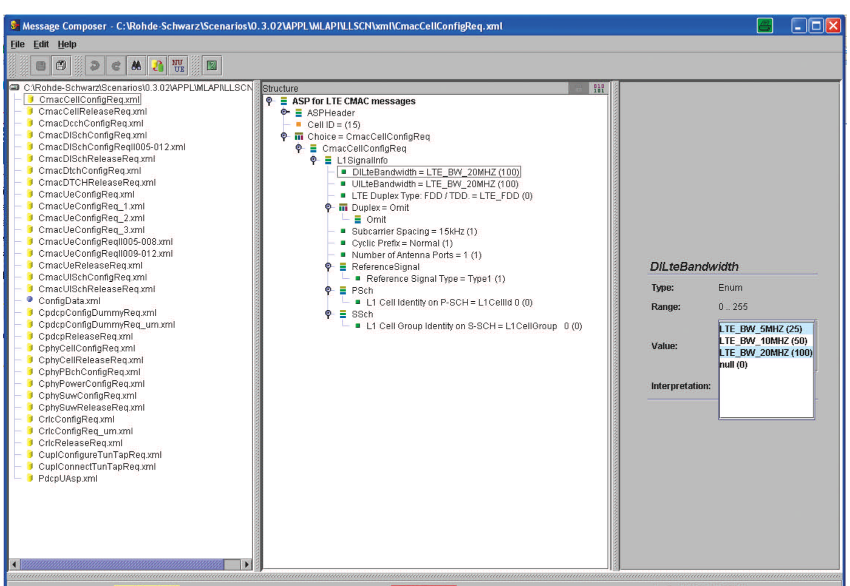

FIGURE 3. A message composer can help you specify the contents of layer-3 messages that are used in a test scenario. These messages can perform functions such as setting up a connection.

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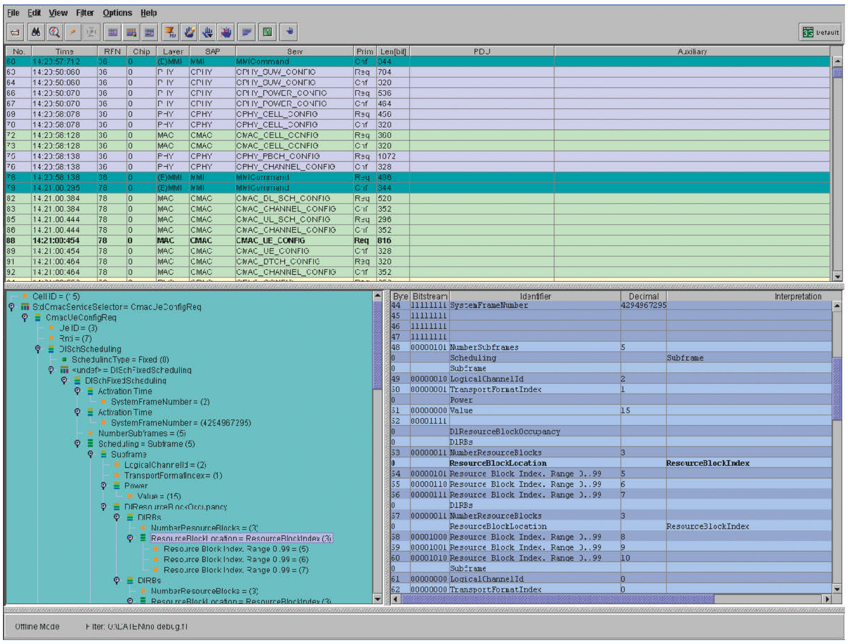

FIGURE 4. A message analyzer can show every message exchanged between the tester and the DUT.

ers can connect the protocol stack to be tested to a virtual tester via an IP connection. LTE test scenarios then verify the behavior of the protocol stack on the wireless device end. These scenarios can include a simple connection setup or more complex reconfigurations. All important functions of the layer-2 and layer-3 protocols can be verified in the virtual test environment of the CMW500, for example.

After layer-1 integration, you can connect the wireless device or chipset to a bench protocol tester for further testing. The connection can take place via RF or in the baseband—for example, over a digital I/Q interface. You can then subject the device under test (DUT) to the LTE test cases to study the behavior of the device and detect possible errors.

When moving to the hardware version of a protocol tester, developers can reuse the scenarios from the virtual-test environment. The R&S CMW500 for LTE also provides test cases that include layer-1 functionality. Of particular interest are the test cases that require an interaction between the downlink and uplink, such as MIMO or the hybrid automatic repeat request (ARQ) protocol.

For throughput measurements, connection to the user plane—for example, to a video streaming server—is important. Actual user data can thus be processed in the protocol test scenario. LTE devices must be able to work with other technologies, as LTE services will not be rolled out everywhere simultaneously.

Test scenarios for development

When testing LTE devices in R&D, engineers should use a flexible programming language like C++ so they can develop numerous complex test scenarios. A distinction is made between the low-level application programming interface (LLAPI) and the medium-level application programming interface (MLAPI), depending on whether the interface accesses layer 2 or layer 3.

The LLAPI offers users particular flexibility for programming layer 2 of the network simulator. Plus, the LLAPI is available early on as it does not require a layer-3 implementation. (The 3GPP is still working on the specification of LTE layer 3.)

On the other hand, the MLAPI is a particularly efficient method because the user does not have to configure layers 1 and 2 on the tester end; layer 3 handles that automatically. The user only needs to specify the desired sequence of the protocol test scenario, plus the contents of the layer-3 mes-

Abbreviations

3GPP	3rd Generation Partnership Project	PDCP	packet data convergence protocol
ARQ	automatic repeat request	PDN	packet data network
eNB	E-UTRAN NodeB base station	P-GW	PDN gateway
EPC	evolved packet core	PHY	physical
E-UTRAN	evolved UMTS terrestrial radio access network	RB	radio bearer
LLAPI	low-level application programming interface	RLC	radio link control
LTE	long term evolution	RRC	radio resource control
MAC	medium access control	RRM	radio resource management
MLAPI	medium-level application programming interface	S-GW	serving gateway
MME	mobility management entity	TTCN-3	testing and test control notation version 3
NAS	non-access stratum	UE	user equipment
		UMTS	Universal Mobile Telecommunications System

sages, for example, for setting up the connection.

Figure 3 illustrates the use of the R&S CMW500 for LTE instrument for editing messages. State machines allow the scenarios to be set up modularly, so that individual components can easily be reused. **Figure 4**, generated by the CMW500 message-analyzer function, shows every message exchanged between a tester and a DUT.

Interoperability scenarios

The first LTE-capable wireless devices will soon be tested in real networks. To comprehensively prepare for these field trials, producers of chipsets and wireless devices will need to perform interoperability tests to completely test a wireless device in the lab and prepare for all test cases in the field. As a result, implementation errors can be detected early on and surprises avoided. If problems do still occur during the field trial, the scenarios can be reproduced in the lab by using the protocol tester, and the implementation error can then be eliminated from the chipset or wireless device.

3GPP is currently working on test specifications for LTE. In addition to test cases for RF and radio resource management, the 3GPP will develop numerous signaling test cases. These will include layer-2 and layer-3 test cases, as well as NAS test cases. The 3GPP will describe these test cases in testing and test control notation version 3 (TTCN-3). The conformance test cases specified in 3GPP will form the foundation for the certification of wireless devices, ensuring that all wireless devices worldwide comply with the same standards.

LTE involves many technical changes for UMTS. Developers of LTE-capable chipsets and wireless devices must therefore carry out numerous protocol tests to detect errors in the implementation early on, thus saving time and money. The interworking between LTE and other radio technologies will be a particularly important task in protocol testing. T&MW

Christina Geßner *has been a technology manager for mobile radios at Rohde & Schwarz headquarters in Munich since 2004. Her tasks include the development and marketing of the T&M product portfolio for UMTS LTE and HSPA. After completing her studies in electrical engineering with emphasis on radio-frequency engineering at the University of Hannover in 1998, Geßner first worked in the strategic product management of the mobile radio networks division at Siemens in Berlin and Munich.*

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Price: $695. *Signametrics, www.signametrics.com.*

Analyze HDMI audio streams

Audio Precision has added support for testing High-Definition Media Interface (HDMI) 1.3 and Blu-ray audio to its eight-channel APx585 audio generator and analyzer. The option lets you test audio on sink (input) and source (output) devices.

For testing sink devices, the APx585 can generate lossless or compressed audio streams and then analyze the resulting analog output for frequency response, amplitude accuracy, noise, intermodulation distortion, and other parameters. The HDMI option also generates HDMI video streams that you can combine with audio streams to produce a full HDMI signal.

The audio generator lets you produce pulse-code modulated (PCM) audio on up to eight channels at sample rates of 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz with resolution up to 24 bits.

Lossy audio streams operate at 48 kHz, 96 kHz, and 192 kHz, also with up to 24-bit resolution. In addition, the instrument generates Dolby Digital and Digital Surround audio streams over HDMI.

To test source devices, the APx585 with HDMI option can accept HDMI digital streams for a source, decode the audio portion, and perform the same audio measurements as it does for sink devices. The APx585 is controlled from a PC through a USB interface. Software that lets you set up and perform automated tests is included.

Audio Precision, www.ap.com.

Event data recorder integrates F-RAM memory

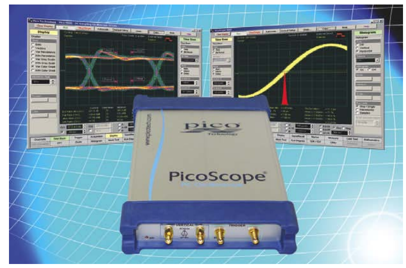
Ramtron International, a developer of nonvolatile ferroelectric random-access memory (F-RAM) and integrated semiconductor products, has launched the FM6124 F-RAM-based event data recorder (EDR). The FM6124 continuously monitors state changes and stores them in the F-RAM. It is designed for use in the industrial control, medical, and metering markets. The EDR can perform in applications including activity, equipment, and environmental monitoring; maintenance scheduling; power-system management; automotive and industrial-automation event recording; vehicle and pedestrian traffic counting; and surveillance systems.

The FM6124 features 32 kbytes of F-RAM memory that can be used to store event records. Up to 24 kbytes of F-RAM can be configured to store event and user data. An on-chip real-time clock (RTC) with calendar enables time stamping of events and can function as a system clock and calendar. The RTC enables further analysis of captured data, which can be used by the system to generate alerts such as an equipment malfunction or a call for maintenance. The EDR includes 12 digital inputs that can be individually configured to trigger event recording on either a rising or a falling edge. The FM6124's F-RAM memory can store up to 4000 event records. The device features an I2C interface that sustains communication speeds up to 100 kbps.

Base price: $7.50 each in quantities of 1000. *Ramtron International, www.ramtron.com.*

A 12-GHz PC-based oscilloscope

The PicoScope 9201 is a two-channel sampling oscilloscope that connects to a PC through a USB port (Ethernet optional). With its 12-GHz bandwidth, the 9201 lets you measure eye diagrams on high-speed serial buses. Waveform analysis includes color-coded persistence. In addition, the instrument produces histograms in either the vertical or horizontal axis so you can measure the distribution of a signal's edge timing or amplitude. You can make eye-diagram measurements and run mask tests on SONET and SDH signals for both return-to-zero (RZ) and non-return-to-zero (NRZ) signals.



In addition to 12-GHz bandwidth, the PicoScope 9201 has 16 bits of vertical resolution. Its scale factors range from 20 mV/div to 255 mV/div. Measurement tools include cursors, channel math (up to four calculated waveforms on the screen at one time), and fast Fourier transforms with a choice of windowing functions. The PicoScope 9201 includes oscilloscope software that runs on Windows XP or Vista (32-bit versions).

Price: £5995 (approximately $12,000). *Pico Technology, www.picotech.com.*

Xantrex introduces triple-output digital power supplies

Xantrex Technology's 222-W linear XBT programmable bench power supplies serve laboratory and low-power ATE applications. The supplies' channels 1 and 2 provide two 0- to 32-V, 0- to 3-A outputs; an additional output is programmable from 0- to 15-V or 0- to 5-A to a maximum of 30 W. Users can manually adjust the supplies using a keypad and a digital encoder knob. For computer control, USB and RS-232 interfaces come standard, while IEEE 488.2/GPIB and Ethernet interfaces are optional.

The XBT supplies can operate in an isolated mode, in which each of the three outputs operates independently. The supplies also offer a tracking mode, in which channels 1 and 2 provide equal but isolated outputs. In addition, channels 1 and 2 can operate in parallel to act as a single 0- to 32-V, 0- to 6-A output, or they can operate in series to provide a single 0- to 64-V, 0- to 3-A output. Overvoltage and overcurrent protection functions are programmable for each channel. Each supply can store up to 100 voltage and current settings.

Base price: $1495. *Xantrex, www.xantrex.com.*

Hipot wire harness tester

Offering the same accuracy and ease of use as the NX line of low-voltage wire harness testers, the NX hipot tester from Dynalab handles high-voltage testing of cable assemblies and wire harnesses.

Available in configurations ranging from 64 to 1024 test points, the new tester performs insulation resistance tests up to 1 GΩ and dielectric withstanding tests up to 1500 VDC. The unit prints a product label only when the wire harness passes all tests. It also restricts an operator from altering the test program and alerts the operator if the wire harness is removed before the test is complete.

The NX tester's memory card is accessible from a PC using a USB adapter, enabling test programs to be downloaded from the PC directly to the memory card. You can also connect to a network for program file transfers and data collection.

Base price: $3695. *Dynalab, www.dynalabtesters.com.*

Sensor captures vehicle crush zone data

Intended for vehicle crash testing, the Model 7287 crush sensor provides certified reliable, predictable performance in terms of several key parameters and avoids the need to characterize the sensor before use. Applications include on-vehicle locations such as bumpers, fenders, doors, and trunk lids, which are likely to be heavily damaged during testing. Since data gathered from these crush zones is critical, sensor reliability is crucial.

The Model 7287 is specified to maximum or minimum values of key parameters, not to typical values. A POP calibration data sheet is provided with sensitivity and full-scale range information.

The Model 7287 accelerometer requires an excitation voltage of 10 VDC and delivers output sensitivity of 0.10 mV/g. It also offers a full-scale range of ±2000 g with a frequency response of 0 to 4000 Hz and resonant frequency of 20,000 Hz. The device features a rugged PVC-jacketed cable that is less than 2 mm in diameter. Three form factors are available: two with the cable and one without the cable.

Endevco, www.endevco.com.

Test system supports all A-GPS test cases

Spirent Communications announces that its UMTS Location Test System (ULTS) now offers full certification testing of the 3rd Generation Partnership Project's (3GPP's) Assisted GPS (A-GPS) RF Minimum Performance test cases for both W-CDMA and GSM devices. Spirent claims it is the first test-equipment vendor to support all A-GPS testing standards, including RF performance, signaling conformance, and Secure User Plane (SUPL) Application Enabler.

The Spirent ULTS enables mobile operators and manufacturers offering W-CDMA devices to certify 100% of the 3GPP TS 34.171 A-GPS RF Minimum Performance test cases. ULTS had already validated five of the six TS 34.171 test cases and now supports certification testing of the sixth test case—Fine Time Assistance (FTA).

Spirent Communications, www.spirentcom.com.

Power amplifier delivers 40 kV

In addition to an output range of 0 to ±40 kV DC or peak AC and an output current range of 0 to ±15 mA DC or peak AC, TREK's Model 40/15 power amplifier provides DC stability, high speed, and precise control of output voltages to meet the needs of a diverse range of industrial and research applications.

The Model 40/15 is configured as noninverting with a fixed gain of 4000 V/V. A potentiometer allows DC offset adjustment over the entire voltage output range. The instrument also features a solid-state design for high-slew-rate, wide-bandwidth, and low-noise operation. The four-quadrant, active output stage sinks or sources current into reactive or resistive loads throughout the output voltage range. DC accuracy is better than 0.1% of full scale; slew rate is greater than 350 V/µs.

TREK, www.trekinc.com.

Simulate and develop wireless systems

Communications Blockset 4.0 extends Simulink from The MathWorks by adding code generation for simulating and designing the physical layer of wireless systems such as WiMAX. Using software blocks that work within the Simulink modeling environment, you can model physical-layer characteristics such as interleavers, filters, and modulators.

Communications Blockset 4.0 also lets you model random integer and binary generators, PN and Gold code sequences, and sinks. You can run error-rate calculations, model eye diagrams, and produce constellation plots.

The software also integrates with Matlab where you can perform post-simulation analysis. A visualization tool within Communications Blockset 4.0 lets you analyze time-varying communications channels.

Base price: $1000. *The MathWorks, www.mathworks.com.*

300-MHz PXI, PCI, and VXI oscilloscopes

Comprising models with two or four channels, the ZT4210 series of 300-MHz oscilloscopes from ZTEC Instruments comes in PXI, PCI, and VXI versions providing the same triggering, math, and analysis functions commonly found in ZTEC's other M-class oscilloscopes.

In addition to an analog bandwidth of 300 MHz, the scopes offer real-time sampling rates of up to 1 Gsample/s (interleaved) and 500 Msamples/s (noninterleaved) with record lengths of up to 256 Msamples. Onboard processing allows the ZT4210 series to calculate more than 40

waveform parameters related to voltage, time, and frequency characteristics. The scopes also come standard with four calculation channels for performing basic and advanced math on acquired data.

The two-channel scopes are available in PXI, PCI, and VXI form factors, while the four-channel model comes in VXI only. All models accommodate direct inputs of ±300 V pk (CAT II). With input ranges from 1.25 mV/div to 40 V/div (10 vertical divisions), the ZT4210 is capable of handling a wide range of voltage levels without the need for external signal conditioning.

Base price: $4450. *ZTEC Instruments, www.ztecinstruments.com.*

Lock-in amplifier boasts low noise

The Model 7124 lock-in amplifier from Signal Recovery provides an all-analog front-end remote connection unit (RCU), to which signal and reference connections are made, and a DSP main instrument console connected via a fiber-optic link. In normal operation, there are no digital clock signals within the RCU, so it emits no switching noise. This architecture gives the advantages of DSP technology for signal detection as well as the low-noise performance that the company claims is typically available only in instruments of all-analog design.

The 7124's main console is a compact bench unit with a color display and keys for operating the instrument controls, accessing different menus, and entering numeric values. It receives signals from the RCU module and processes them using DSP algorithms running in a dedicated FPGA supported by a ColdFire processor.

The amplifier has an operating frequency range of 0.5 Hz to 150 kHz with a main ADC sampling rate and analog output DAC update rate of 1 MHz. The Model 7124 also provides output filter time constants ranging from 10 µs to 100 ks.

Signal Recovery, www.signalrecovery.com.

MACHINE-VISION&INSPECTION

TEST REPORT

Complex circuits challenge cameras

By Steve Scheiber, Contributing Technical Editor

As designers continue to propose ever-smaller, ever-more-complex circuits, the demands on inspection equipment push the limits of what today's cameras can provide. Bruce Butkus, product line engineer for Edmund Optics, offered his observations on the resulting challenges.

Q: What do you regard as the most significant issue facing the inspection industry?

A: Being able to see all of the circuit's features in enough detail despite higher production volumes. Manufacturers of mobile phones and automotive electronics, for example, don't want any defects. Yet, as the components get smaller, the defects get smaller as well. You end up pushing the limits of camera performance.

If you raise the resolution, you necessarily reduce the field of view. At twice the resolution, you can only cover a quarter as much area, so you need four times the number of images.

Q: How can you capture that number of images without compromising throughput?

A: You can add more cameras to the inspection system or you can make the same number of cameras work faster. But for one camera to capture more images in a period of time, you have to reduce the exposure time, reducing the time during which light gets through the lens.

That, in turn, requires rethinking lighting schemes. In fact, proper lighting becomes one of the critical issues. The lights have to be brighter to start with.

In addition, a board featuring highly complex geometry that includes components of different sizes and heights, different shapes of solder paste, and other irregularities poses a complicated environment to achieve adequate lighting. You can use software to enhance the images and thereby increase the level of detail, but generally not fast enough to do it on the fly.

Q: Is resolution the limiting factor?

A: We're definitely approaching the fuzzy edge of what camera designs can deliver. We can specify adequate performance on paper, but manufacturing real cameras that can achieve that level of performance is becoming more and more difficult.

The technology of television-class resolution hung around for 50 years. The newest tools have increased that resolution by a factor of 20 in barely eight years. We can't increase resolution by another order of magnitude without making major compromises in other performance parameters, and certainly in cost.

Bruce Butkus
Product Line Engineer
Edmund Optics
Courtesy of Edmund Optics

Q: Are customers who are looking for this optimum performance still so cost-conscious?

A: Part of the problem is perception. There is a vast price difference between a consumer-grade camera and an industrial-grade camera that delivers the same specifications. You can walk into any electronics retailer and get a certain specification camera for, say $150. But the consumer product is designed for casual photography and occasional light use.

A comparable industrial-grade camera designed to work reliably and unattended in a manufacturing line would be priced more than an order of magnitude higher. Like the consumer models, these cameras have also undergone substantial price erosion in recent years. A few years ago, that camera might have cost $80,000. Industry experiences the same price erosion as the consumer world, but from a much higher starting point. □

INSIDE THIS REPORT

EDITOR'S NOTE

Looking through inspection's crystal ball

Steve Scheiber, Technical Editor

Inspection techniques have clearly become an essential part of "test." X-ray inspection, once relegated to the sidelines of sampling and spot-checking, has been pushed to the forefront by ball-grid arrays and other hidden-node architectures. Automated optical inspection emerged to reduce inconsistencies in manual techniques caused by operator fatigue and by ever-smaller inspection targets.

But inspection, too, has its limitations. The tradeoff between resolution, field of view, and speed becomes more serious as circuits get smaller and more crowded, and constant price erosion increases the clamor for higher throughput and reduced costs. Proponents of today's techniques can't make the mistake of becoming complacent.

New semiconductor materials, organic circuitry, and other breakthroughs will eventually push both inspection vendors and test strategists to find creative new solutions. One recent example was an announcement last month by Hewlett-Packard about the creation of *memristors*. These alternatives to transistors, first proposed more than 30 years ago by Professor Leon Chua at UC Berkeley, will dramatically shrink logic once again, yet will retain their information even when power is off.

"We've always done it that way" has never sufficed to meet tomorrow's technology challenges. We always have to look forward. □

Contact Steve Scheiber at sscheiber@aol.com.

HIGHLIGHTS

Carl Zeiss SMT opens headquarters

At what the company billed as "the smallest ribbon-cutting ceremony in history," Carl Zeiss SMT opened its North American headquarters in Peabody, MA, on April 23. The new facility houses engineering, manufacturing, and technical support. Products include scanning-electron microscopes, crossbeam microscopes, and helium-ion microscopes.

Speaking to the invited audience during the ceremony, company president Frank Averdung explained that the Carl Zeiss instruments can measure distances "from stars to atoms." The ceremony also included a video presentation, "The world's smallest ribbon cutting," that showed an image of a blue ribbon from a high-power microscope as a beam cut the ribbon. www.smt.zeiss.com.

YesTech automates coating inspection

YesTech has introduced a B-UV conformal coating inspection system that automates the process of using ultraviolet lighting for determining the quality, consistency, and thickness of conformal coatings on electronic products. The B-UV system can identify delamination, cracks, and bubbles as well as areas of noncoverage.

YesTech reports that system setup can typically be completed in only a few minutes, as the B-UV uses a known-good board to learn the coverage and noncoverage areas. Subsequently, the automated inspection typically takes only a few seconds. Results can be immediately displayed or can be stored for later review. The B-UV reads all common bar codes to support product traceability, and an optional software upgrade enables the system to determine component presence and location. www.yestechinc.com.

Fiber-coupled laser maintains stable temperature

The single-mode fiber-coupled Lasiris PureBeam laser from StockerYale employs a thermoelectric cooler to maintain a constant laser diode temperature, improving the stability of both wavelengths and output power, according to the company. The PureBeam laser covers a wavelength range of 375 nm to 830 nm and delivers output power of 1 mW to 60 mW. All models emit diffraction-limited circular beams.

For applications requiring uniform flat-top illumination, the PureBeam

Learn about machine-vision lighting

Increasing machine-vision resolution to inspect ever smaller circuit features triggers the need for increased frame rates to maintain production throughput. Higher frame rates, in turn, require decreased exposure times. Capturing images of sufficient quality with shorter exposures demands adequate lighting of the objects under inspection.

To help you illuminate your products properly, National Instruments has posted three tutorials to its Web site that cover the topic of lighting in machine-vision systems. The first article in the series, which was written by Daryl Martin of Advanced Illumination, introduces the basic concepts and theories of inspection lighting. It provides information about the types of lighting available and the optimum arrangement of lighting sources.

The other two articles in this series (which actually appeared on the Web site first) explore various lighting techniques and describe how to design an efficient lighting system. zone.ni.com/devzone/cda/tut/p/id/6901.

laser can be integrated with the company's Flat-Top2 Generator, a beam-shaping module that converts a Gaussian beam to a flat-top square or rectangular profile. The PureBeam laser is designed for applications such as machine vision, confocal microscopy, and industrial inspection as well as spectroscopy and fluorescence. www.stockeryale.com/lasers.

16-Mpixel camera gains GigE interface

A high-speed version of SVS-VISTEK's 16-Mpixel svs16000 industrial CCD camera integrates a Gigabit Ethernet interface to achieve a frame rate of 4 fps at a resolution of 4896x3280 pixels. The svs16000-U is the first member of the SVCam-CP family to offer the GigE interface. The progressive-scan svs16000-U is available in both monochrome and color versions. www.svs-vistek.com.

Applied Materials introduces mask inspection system

The Applied Aera2 mask inspection system from Applied Materials uses aerial imaging technology to reveal how the pattern on a mask will appear on a wafer. The company claims that the system detects defects according to their impact on the wafer, and it filters out nonprinting defects.

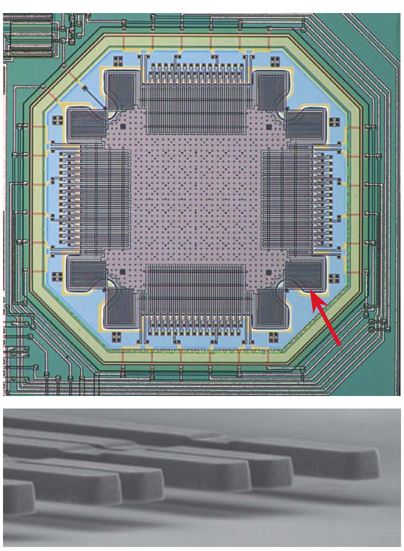
Applied Materials explains that by emulating the optical system of 193-nm lithography scanners and placing an image sensor in the wafer plane, the Aera2 system inspects the mask under the same optical conditions as when it is exposed in a stepper to provide "what you see is what you print" capability. An optional application uses the imaging data to create uniformity maps of an entire mask. These maps can reveal subtle manufacturing effects to help mask makers fine tune the mask manufacturing process. www.appliedmaterials.com.

MEMS create 3-D inspection challenges

By Jon Titus, Contributing Technical Editor

Microphones, accelerometers, pressure sensors, and many other products take advantage of a microelectromechanical system, or MEMS, crafted on a wafer of silicon. The diversity of MEMS devices presents vendors and users of inspection system with a sizeable challenge: Unlike integrated circuits that all look somewhat similar, each MEMS device has its own peculiarities and structures that require a unique inspection "recipe."

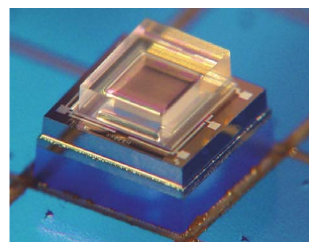
For example, an ink-jet printer cartridge uses a MEMS to electrically heat the ink and spray it onto paper through a precision opening—the jet. If process steps produce malformed, partially blocked, or fractured jets, a cartridge will not work properly, but only careful inspection of a MEMS wafer will detect these problems. Optical inspections also can measure the jet openings and identify blocked jets, foreign material in jets, and misshaped orifices.



(Top) The sensor portion of an ADXL202E dual-axis accelerometer measures deflection of a MEMS differential capacitor that comprises independent fixed and central plates attached to a moving mass. The red arrow points to one of the eight springs that hold the mass in place. (Bottom) This image shows details of the sensor "fingers."

Courtesy of Analog Devices.

"Compared to MEMS inspections, inspection of semiconductors was easy," said Rob O'Reilly, test-development manager at Analog Devices, a manufacturer of MEMS accelerometers. "One inspection system will inspect a variety of semiconductor wafers. But you cannot buy one piece of equipment and realistically expect it to optically measure and inspect several types of MEMS products on a production line. So, MEMS inspections cost a bit more, but when MEMS devices go into a safety-critical product such as an airbag sensor, you must inspect every one. You cannot simply inspect samples from a batch."



A glass cover hermetically seals a MEMS pressure sensor on a substrate. Manufacturers apply a large glass plate on a single wafer and then saw the glass to isolate individual sensors.

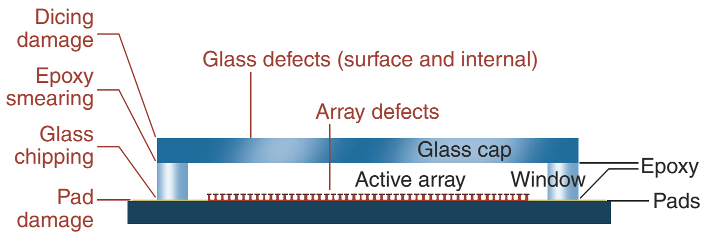
Courtesy of Intersema and Camtek.

"We look at semiconductor wafers for discoloration, cracks, and other defects to determine if a problem occurred during the fab processes," explained O'Reilly. "But with accelerometer MEMS wafers, we must look at the sensor electronics and at the micromachined mechanical beams to ensure the etching processes 'released' the beams, that they have uniform dimensions, and that the dimensions meet our requirements."

A typical MEMS device includes structures at different heights, so some components rise a few microns to tens of microns above others. "Test engineers who inspect MEMS dice need a system that can focus at different levels," said Rajiv Roy, marketing director for inspection at Rudolph Technologies. "An engineer might say, 'I found a defect deep down in the middle of a channel, but then I found another defect high up on a structure, and I want to see both.' If your system cannot focus at different levels in an adaptive way, you may get a good view of the higher defect but the defect low in the channel looks out of focus. A MEMS inspection system should have the capability to capture high-quality images no matter where a defect lies on the MEMS topography."

"Many MEMS devices contain 3-D structures. Most inspections of these structures can be performed by taking one single image. To inspect a structure for a 1-micron defect, for example, a camera may have to perform inspections at different heights due to its limited depth of focus at very high magnifications," noted Pieter Vandewalle, director of sales and marketing at ICOS Vision Systems. "Besides, test engineers may want to measure 3-D structures on the die as well. The capability of some 3-D metrology tools lets test engineers take one image and get a 3-D profile of a complete MEMS die. Then, a customer can decide what dimensions to measure and how to use the dimensional information. They might need an absolute height or perhaps they only need to know a component's height is less than *x* microns. These types of requirements differ greatly from customer to customer."

Because MEMS rely on precisely formed mechanical components,



This cross-section diagram of a generalized MEMS device indicates the locations and types of possible defects that require optical inspection.
Courtesy of Camtek.

measurement of critical dimensions plays a key role in inspections. Pressure-sensor and accelerometer MEMS devices manufactured by Freescale Semiconductor rely on precision springs. "We must measure critical dimensions of the springs, but when we used traditional wafer-inspection equipment, the MEMS die looked huge by comparison," said Hemant Desai, Freescale's MEMS development manager. "Typical MEMS springs may measure two microns or larger, but the usual semiconductor inspection 'tools' measure characteristics on the order of 500 angstroms, or half a micron. Thus, we had to adapt the tools so we could use them to measure critical dimensions on large MEMS structures."

Inspect all aspects of MEMS dice

Because MEMS devices include microscopic moving parts, manufacturers cannot simply mold hot plastic on top of them as they would a standard IC. "Instead, they sandwich them in several layers of silicon or glass," explained Amir Gilead, VP of semiconductor inspection products at Camtek. "Vendors use glass with optical MEMS devices, where it must protect the device from the environment and retain good optical properties. In this type of device, you must inspect the top glass layer for stains and scratches, the edges for dicing damage and cracks, the glass medium for bubbles, the interface between layers for void-free bonding, the periphery for glue or glass-frit residue, and the exposed electrical pads on the active silicon layer for probe-mark damage or contamination. Then, you must inspect the integrity of the active MEMS area through the glass." To further complicate things, each inspection may require a different focus, magnification, illumination, and analysis algorithm.

In addition to mating a MEMS wafer and a cover wafer to protect individual sensors, Analog Devices puts some MEMS sensors in open-cavity ceramic or plastic packages. A lid hermetically seals the sensor inside. "You constantly hear about particle contamination within the MEMS industry," said O'Reilly. "During MEMS production, we worry about micron- and submicron-size particles. No one wants those particles in airbag sensors. So, when we use open-cavity packages, we inspect for residues or particles on the lid and in the package cavity before we insert a clean die. Those particle inspections are critical for hermetic packaging, and they are the most intensive inspections we do. Simultaneously, we perform metrology measurements that determine die tilt, die rotation, and alignment of the package and the die. We inspect every device during these steps."

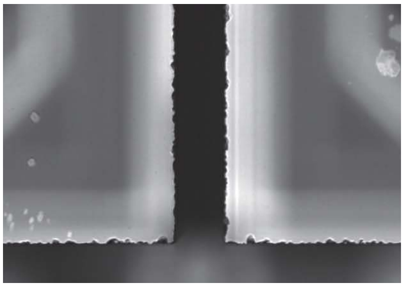
Accept variations within limits

Not all defects or process variations carry the same weight in a MEMS device. "Engineers might see slight changes in the characteristics of MEMS ink jets," explained Rudolph's Roy. "The etching process might not offer the same repeatability as expected from a semiconductor-process-

MEMS challenges • from page 65

ing line. Perhaps a MEMS feature 'moved' slightly or its shape changed slightly. A standard inspection system would sense these small changes as defects, while a customer might find them within spec for the type of product a MEMS device will drop into. Hence, an inspection system should have the flexibility to prioritize defects by regions of interest."

He added, "When you have two operators examine the same group of wafers, they will agree on many defects but disagree on some small quantity. So, engineers should not expect an inspection system with automatic defect-classification [ADC] software to offer 100% accuracy. We recommend customers use ADC software to automatically classify the defects everyone agrees on, which reduces manual-inspection expenses. Then, customers will use ADC capabilities to classify a small set of 'questionable' defects as a consistent referee or to give equipment operators an easy way to manually review defects."



After a saw cuts through the glass covers on MEMS devices, an inspection shows the jagged glass edges as well as defects on or in the glass covers. Courtesy of Camtek.

Surfaces complicate inspections

The thicknesses of deposited polysilicon layers can add to inspection challenges. "Yet, thickness is a critical factor in determining how well a MEMS device will work," explained Freescale's Desai. "But when you deposit polysilicon to a depth of two to five microns, the surface gets rough and it complicates thickness-measurement methods that rely on optical or ellipsometry techniques. A rough surface has a low optical 'signal-to-noise ratio,' which decreases measurement accuracy. We had to put a lot of effort into developing techniques that improved the accuracy of thickness measurements." Equipment vendors also have techniques that improve on polysilicon thickness measurements.

"Vertical, or bright-field, illumination produces good images of flat surfaces," noted Udi Efrat, strategic marketing manager at Camtek. "Angled, or dark-field illumination, accentuates structures and a mechanical defect such as a scratch. Because MEMS devices contain a mix of surfaces and 3-D structures, the inspection system

Inspect MEMS Offline

To characterize and test MEMS dice and devices, technical people in failure-analysis and quality-control labs need something other than a production-line vision system: They require instruments that make measurements from the atomic level up to the level at which they can perform noncontact optical inspections of an entire MEMS device. A typical lab might use an atomic-force or scanning-probe microscope to measure atom-scale dimensions, a stylus profiler for larger dimensions, and an optical profiler that provides accurate surface topology information about MEMS structures.

"People often use a prober to examine dice on a wafer before they go to the expense of putting them in costly packages," explained Erik Novak, director of research and applications at Veeco Instruments, a supplier of optical, stylus, and atomic-force metrology systems. "Then, after they package known-good devices, they inspect them again. Optical profilers let them 'see' MEMS devices they have encapsulated under glass or another transparent material. They might need to acquire the surface profile of a packaged micro-mirror array used in a projection TV set."

Inspections also can provide information about the dynamic operation of MEMS devices under operating conditions. "Suppose you have a MEMS resonator that slides back and forth. We can characterize it at every point in its motion and provide a 3-D map and quantitative analyses that let analysts know if it tilts out of its plane or if it experiences motion perpendicular to its intended direction of travel," said Novak. "In addition to looking for the usual types of defects in MEMS, lab people inspect interface boundaries, material grains, effects of friction and wear, and surface roughness, among other characteristics."

MEMS manufacturers continue to hear that reliability prevents MEMS devices from taking over from traditional technologies. "People know their bulky gyroscopes and analog circuits work almost forever," noted Novak. "So, MEMS devices must offer OEMs lower costs and higher reliability." To test reliability, engineers will put MEMS devices in environmental chambers and cycle them from –200° to +200°C. And they will monitor how the devices behave in real time. They cannot do that sort of testing with production inspection systems.

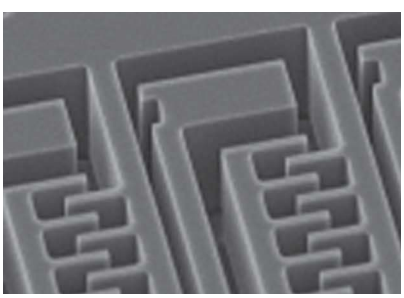
MEMS devices include membranes, mirrors, resonators, gyroscopes, accelerometers, and so on. So, inspection software must recognize vastly different types of features in an image and divide an image into segments. Then, researchers can automatically track the motion of several things in a field of view.—*Jon Titus*

For three short videos that show dynamic MEMS devices as seen by Veeco Instruments' Wyko DMEMS 1100 optical profiler, go to the online version of this article at www.tmworld.com/2008_06.

should balance bright-field and dark-field illumination." For best results, an inspection system should provide programmable light settings based on the MEMS device being inspected. The combination of the two light sources produces good contrast between defects and the background.

Roy explained that because features and surfaces on MEMS vary so widely, his company developed an illumination toolkit. "The kit lets test engineers select from 10 types of filters and light sources so they can adjust the inspection system for a variety of applications."

ICOS tackles inspection of surface defects in two ways. "First, we can use dark-field illumination, colored lights or oblique illumination from



The bottoms and sides of the channels and plateaus in a MEMS sensor all require inspection, so a vision system must change its focus to capture images of defects at all levels.
Courtesy of Freescale Semiconductor.

ring lights," said Vandewalle. "Each material reflects colors differently, so by using one color for illumination, our system can highlight specific materials in an image and de-emphasize others. In this way, users can more easily focus on a gold layer, for example, to determine that it is evenly distributed and not damaged." Second, ICOS provides algorithms that distinguish between defects and the optically "noisy" background of a rough surface.

Making things even more interesting, some wafers need their back surface inspected as well. "Consider a pressure-sensor wafer, which has a thick base layer of perforated silicon bonded to its back surface," said Camtek's Efrat. "The orifices in the base layer should align with the center of each sensor die, and orifices must be open to conduct pressure to the membrane. The orifices should be smooth and have precise dimensions so they properly fit and seal to the sensors. The inspection system will verify the orifices meet specifications and report deviations. And the inspection system must match any defects on the back surface to the corresponding MEMS dice on the front side."

Handle wafers with care

When you plan to inspect MEMS wafers, be sure to address how inspection equipment will handle them. "A standard inspection system uses a vacuum chuck to hold wafers in place," explained Efrat. "But if the silicon substrate has small holes through it, as in the case of the base wafer for MEMS pressure sensors or the windowed glass substrate for an optical MEMS device, a regular vacuum chuck will not work. The inspection system vendor should produce a special chuck or an adaptor to secure a perforated wafer only around its perimeter.

"To inspect an upside-down wafer of pressure sensors, for example, you must protect the MEMS devices on the front side from rubbing against the chuck's surface. We supply a chuck with a recess and apply vacuum only along the wafer's perimeter only to hold it in place without damaging the MEMS structures."

Inspecting MEMS wafers and dice requires you to think about new types of defects, critical dimension measurements, inspections of different horizontal levels, issues with surface effects, and new ways to handle wafers. Unfortunately, MEMS designers often don't think about inspection until they are ready to manufacture a device. Thankfully, vendors have given the topic much thought and can help you determine how to properly inspect your MEMS wafers. □

Where to put AOI?

Steve Scheiber, Contributing Technical Editor

Ever since automated optical inspection (AOI) became a mainstay of a manufacturer's test strategy, planners have debated where to place it in the production process. Do you inspect the solder paste before component placement, inspect the component presence and position after placement and before reflow, inspect the entire board after reflow, or perform some combination of these steps?

To help sort out the advantages and disadvantages of these alternatives, Pamela Lipson, CEO of Imagen, and Lyle Sherwood, VP and director of technology for Landrex Technologies, collected data about defects from several customers of Landrex's AOI systems. They then conducted a study with one customer, a manufacturer of high-volume, high-complexity boards, in which they inspected boards at post-placement, repaired the post-placement defects, and inspected the boards again at post-reflow.

The study let them compare the benefits of post-placement vs. post-reflow AOI. Lipson presented their analysis at April's APEX show in Las Vegas. She subsequently explained the results to me in an exclusive interview.

"We worked with both OEMs and contract manufacturers with a wide range of volume, mix, and complexity," explained Lipson. "In the data we captured with both types of users, the greatest number of defects resulted from post-placement defects, including misinstalled parts and missing parts."

Lipson said that they did not examine the value of using AOI at the post-solder-paste stage, "because most of the customers we surveyed do some inspection at that point anyway. They use it to detect gross problems, such as stencils that need cleaning." She continued, "Generally, post-paste inspection results in a go/no-go decision. That is, the manufacturer doesn't repair portions of the board, but wipes it clean and returns it to the beginning of the process. Post-paste inspection can predict some future defects, but post-placement can often find those defects as well. Therefore, we regard it [post-paste inspection] as orthogonal to post-placement or post-reflow inspection. Thus, we focused on the latter two inspection steps."

Lipson explained that the boards in the study used primarily lead-free solder. She noted that the reduced wetting characteristics of lead-free solder (compared to leaded solder) make it less likely that a placement problem will resolve itself in the reflow oven.

Finding the best place to position the AOI system is crucial to a manufacturer's ability to adjust the production process properly. Conventional wisdom, Lipson acknowledges, says that the earlier in the process you inspect parts and correct process flaws, the more money you can save.

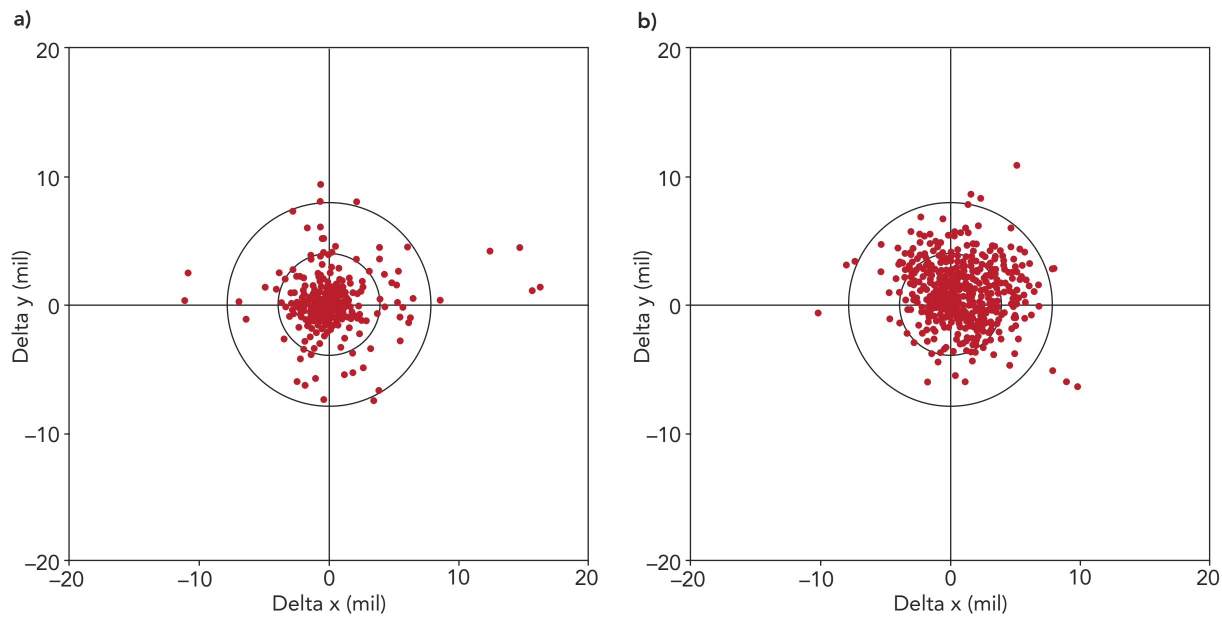


Fig. 1 These post-placement scatter diagrams show component placement accuracy on two different production lines. Although the number of components that exceed the 8-mil gross defect limit is comparable, the number of "marginal passes" in b suggests that the machine is on its way to producing a greater number of gross defects and therefore needs adjustment. Courtesy of Landrex Technologies.

"Defects uncovered before reflow cost less to repair than those found later," she said. "In addition, post-placement AOI generally occurs in-line with production in real time, so any process-related defects can be identified immediately and the process corrected. Post-reflow, on the other hand, is often applied to board batches that come off the line during a certain period of time. If a defect goes undetected until that point, the process will likely create many more defective boards before correction."

Yet, Lipson noted that the stage at which AOI is used is sometimes chosen for logistical reasons rather than technical or economic ones. "Process groups," she explained, "are often responsible for post-placement AOI, for example, while the responsibility for end-of-line AOI rests with test groups. Members of each group naturally prefer the solution that belongs to them."

Post-placement seems best

Through their research, however, Lipson and Sherwood concluded that performing AOI at post-placement provides the best opportunity to catch the greatest number of defects and repair any process problems. "Post-placement inspection can uncover some *design* issues as well," Lipson said. "In one case, a complex component had larger end pins than center pins, yet the board pads were all the same size. That mismatch produced a lot of post-reflow defects that simple post-paste inspection can never find. Analysis of only the joints without looking at the part relative to the pads will obscure this condition, and the root cause will go undetected."

Lipson and Sherwood also found that waiting until post-reflow to perform inspection can lead to some misdiagnoses and, consequently, incorrect adjustments to the production process. "Our research showed that many placement-related defects get incorrectly diagnosed at post-reflow AOI," Lipson said. "A grossly misplaced component can manifest as tombstoned or billboarded after reflow. Accurately determining the source of a defect increases the success of process adjustments made in response."

She also explained that there are other placement defects that can be correctly diagnosed only through post-placement inspection: "If the placement machine pushes too hard when inserting a component, a post-placement inspection can detect deformation of the solder on the pad. Post-paste inspection will not detect a problem, because at that point, no problem exists. After reflow, the defect would show up as a solder bridge. If paste is applied correctly and the component is deposited correctly, the oven itself can't cause such a defect."

Lipson added, "Post-placement inspection can also indicate when placement machines need adjustment before the process produces any defective boards." **Figure 1** shows the placement position for all components on a single board type on two production lines. Lipson explained, "Parts within the 4-mil circle generally indicate an accurate placement, while components placed more than 8 mils from the ideal position constitute 'gross defects'. Although both lines show a few such gross defects, the placement machine in Figure 1a demonstrates a much tighter profile than Figure 1b, suggesting that without adjustment, any further drifting of component positioning from the machine in Figure 1b will generate numerous defects. Again, the reflow oven may obscure the situation, and post-reflow—which focuses on solder joints and gross placement defects—may not detect such placement trends. Thus, without inspection post-placement, the need for adjustment will not be noticed until after a significant rise in the number of defective boards."

Lipson concluded, "At one point in the study, we repaired all defects that the pre-reflow inspection step found to determine how many more defects would show up at post-reflow. We found—somewhat to our surprise—that virtually *all* the defects on those boards could have been detected or repaired before the board entered the reflow oven." □

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VIEWPOINT

[An exclusive interview with a technical leader]

ANTUN DOMIC
Senior VP and GM
Implementation Group
Synopsys
Mt. View, CA

Joining Synopsys in 1997, Antun Domic now manages the Implementation Group, which is responsible for the company's flagship synthesis and physical design products, test automation, signal integrity, power analysis, and timing and formal verification products. Before joining Synopsys, he worked at Cadence Design Systems, Digital Equipment, and MIT Lincoln Laboratory. Domic holds a PhD in mathematics from the Massachusetts Institute of Technology and a BS in mathematics and electrical engineering from the University of Chile.

Contributing editor Larry Maloney conducted a phone interview with Domic on the role of design for test in curbing costs and ensuring reliability in IC design and manufacture.

How DFT conquers chip complexity

Q: Is design for test (DFT) strictly the domain of DFT engineers?
A: Certainly, there are DFT specialists, and their responsibility is to construct the DFT strategy for the chip. But verification engineers also need to understand DFT, since they must verify the chip functionality in its test mode. As for design engineers, we see that users of our Design Compiler tool—traditional logic design engineers—also run DFT Compiler and DFT MAX, our scanning and compression tools. We've made these tools part of the design flow, so these engineers don't have to call in test experts.

Q: What impact is growing IC complexity having on test?
A: One example is that you can have a path with no defects from the standpoint of functional failure. An increased resistance on a via will make the node switch, but the delay is going to be much longer, resulting in a small delay defect. Another growing concern is power consumption. As engineers reduce power consumption on chips, they are designing thinner power and ground lines. As a result, testing can stress the chip with an amount of switching that can cause a failure. So, a new challenge is how to keep the pattern count low and the coverage high while reducing power consumption.

Q: What are your key tools for addressing new test challenges?
A: Our DFT MAX automatically implements "adaptive scan," the Synopsys version of scan compression, on chip hardware to reduce the amount of test data. Companies need this technology for two reasons: First, testers have a finite amount of memory to retain test patterns, and second, customers want to limit the time spent by the tester on each device. If test patterns exceed the tester memory limit, they are cut back, which lowers test quality, ultimately resulting in higher service costs. You can add memory, but this increases costs. At our San Jose user conference, RFMD, a supplier of wireless components, reported projected savings of $25 million from using DFT MAX.

Q: How about improvements in automatic test-pattern generation (ATPG)?
A: Advanced fault models are driving ATPG to produce higher test quality. For example, small delay defects associated with nanometer processes can adversely affect timing-sensitive paths, leading to circuit failures. Standard transition-delay ATPG lacks sufficient timing resolution to create tests that reliably detect these small delays. The Synopsys TetraMAX solution, however, can process precise timing information from the PrimeTime suite to generate small delay defect patterns and identify subtle defects that were previously undetectable.

Q: Moving forward, what will be your key focus in DFT technology?
A: Early this year, we announced that our IC Compiler was used in a 45-nm system-on-chip device from Matsushita. The size of this chip was over 250 million transistors. So, customers clearly are planning larger designs. This means we'll need to make more strides in compression to extend tester life.

More gates on the chip also require greater capacity and faster run time, which we're addressing in all our tools, including test. Customers want to reduce power in test-pattern generation. As we move to smaller chip geometries, such as 32 nm, we'll need to respond to defects related to small delays and other issues.

Finally, there's the challenge of design flow. For example, the more compression you do, the more problems you have in place and route because of more congested circuitry. We must always make sure that overall design productivity is not compromised by test requirements. T&MW

Antun Domic addresses more questions on DFT, including regional needs among engineers, in the online version of this interview: www.tmworld.com/2008_06.

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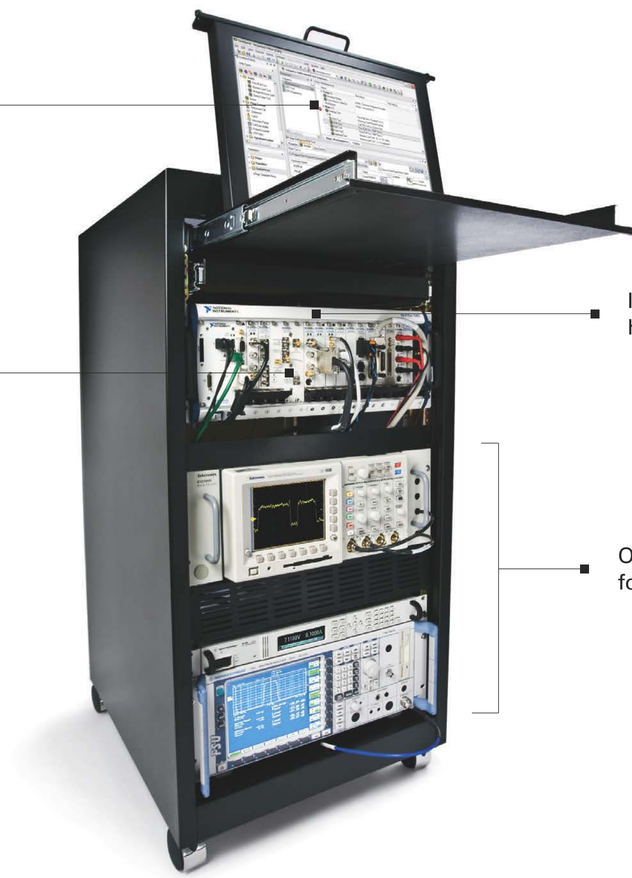

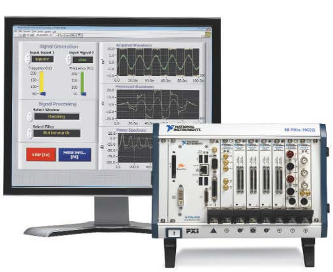

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